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FIELD MAINTENANCE PRINT SET

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TABLE OF CONTENTS

B-TC-6300B-0-DBU	6300B MICRO VAX II WORLD BOX (TC)
D-UA-6300B-0-DBU	6300B MICRO VAX II WORLD BOX
K-PL-6300B-0-DBP	6300B MICRO VAX II WORLD BOX (PL)
B-DD-6300B-0-DBU	6300B MICRO VAX II WORLD BOX (DD ONLY)
B-DD-M7606-0-0	MICRO VAX II CPU (DD ONLY)
D-UA-M7606-0-0	MICRO VAX II CPU
K-PL-M7606-0-DBP	MICRO VAX II CPU (PL)
D-CS-M7606-0-1	MICRO VAX II CPU
B-DD-5416744-0-0	FUNCTION SEL/SLU CONSOLE CONN (DD ONLY)
D-UA-5416744-0-0	FUNCTION SEL/SLU CONSOLE CONN
K-PL-5416744-0-DBP	FUNCTION SEL/SLU CONSOLE CONN (PL)
D-CS-5416744-0-1	FUNCTION SEL/SLU CONSOLE CONN
B-DD-M9047-0-0	Q BUS GRANT CONTINUITY CARD (DD ONLY)
D-UA-M9047-0-0	Q BUS GRANT CONTINUITY CARD
D-CS-M9047-0-1	Q BUS GRANT CONTINUITY CARD
A-PS-1700712-0-0	CABLE ASSY, 20 PIN
A-PS-1700624-0-0	CABLE CONSOLE BACKPLANE
K-PL-7022382-0-DBP	ACCESSORIES KIT
A-PS-1700301-0-0	CABLE ASSY, 7 COND
MP-02049-01	PRINT SET BA123-A BASIC ENCLOSURE

UNIT VARIATIONS COVERED BY THIS PRINT SET

6300B-A2
6300B-A3
6300B-B2
6300B-B3
6300B-C2
6300B-C3
6300B-D2
6300B-D3

6300B FIELD MAINTENANCE PRINT SET

DIGITAL EQUIPMENT
CORPORATION

PRINT SET PART
NUMBER MP-02071-01
REV A1

FILE NAME: TC-6300B-0-DBUA

REVISION HISTORY	DATE	ECO NUMBER	REV.	D. HEALY D. HEALY J. NICHOLS K. WORTMAN FIELD SERVICE TOP DOC. B-DD-6300B-0-DBU	DRN.	DATE	TITLE 6300B MICRO VAX II WORLD BOX		
			A			25FEB85			
						19MAR85			
						19MAR85			
						19MAR85			
						19MAR85			
							SIZE CODE	NUMBER	REV.
					B TC	6300B-0-DBU	A		
					SHEET 1 OF 1				

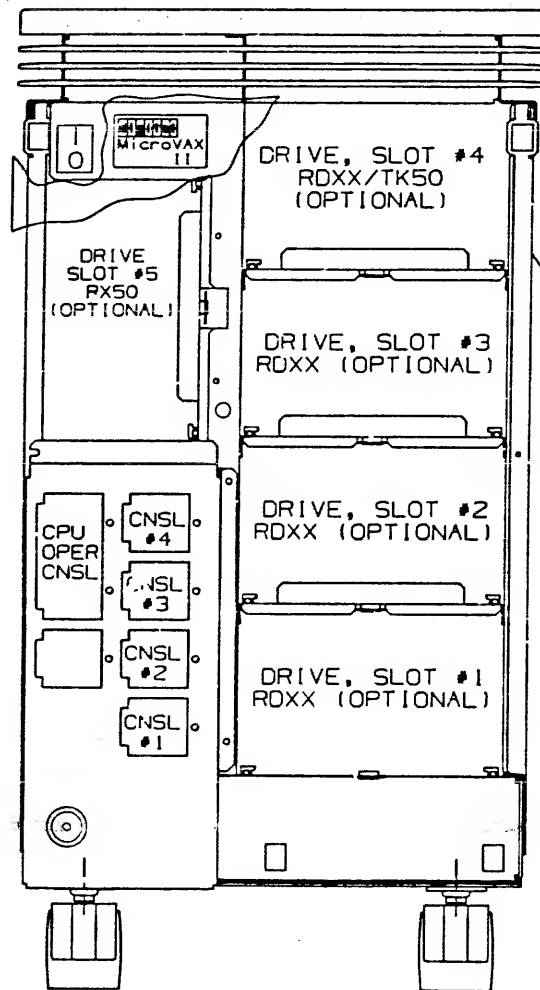
MLO1

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LEGEND		
PART NO.	REV	VARIATION
6300B-A2	A2	1 MB FP 120V
6300B-A3	A2	1 MB FP 240V
6300B-B2	A2	1 MB NO FP 120V
6300B-B3	A2	1 MB NO FP 240V
6300B-C2	A2	256 KB FP 120V
6300B-C3	A2	256 KB FP 240V
6300B-D2	A2	256 KB NO FP 120V
6300B-D3	A2	256 KB NO FP 240V

NOTES:

- BACK PANEL CONFIGURATION RULES & MASS STORAGE CONFIGURATION RULES: REF D-AR-7022380-0-DBU
- ITEM #5 NOT SHOWN ON THIS ASSY.



VIEW A-A
(FRONT)
(SEE SHEET 2)
SHOWN WITHOUT FRONT
OR SIDE PANELS

(SEE SHEET 2)

LAYER #6: WORK LAYER (SHT 4)
LAYER #5: WORK LAYER (SHT 3)
LAYER #4: FORMAT LAYER (SHT 2, 3 & 4)
LAYER #3: WORK LAYER (SHT 2)
LAYER #2: FORMAT LAYER (SHT 1)
LAYER #1: WORK LAYER (SHT 1)
PLOT SCALE: .50
SYSTEM #: 20
PROGRAM VERSION: UGRAF D4.1
FILE NAME: 6300B-0-DBUB
TITLE: 6300B MICRO VAX II WORLD BOX

PLOT AT .50

CAUTION: OFF SHEET PARTS LIST EXISTS
REFER TO K-PL-6300B-0-DBP
(ML 863)

DESCRIPTION		DRAWING NO.	PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND THE FOLLOWING TOLERANCES APPLY (PER DEC STD 114)				
DIMENSIONS	INCHES	DIMENSION RANGE IN INCHES		
	TOLERANCES	OVER 0.2 TO 1.0	OVER 1.0 TO 12.0	OVER 12.0 TO 40.0
ANGLES	± .02	± .02	± .03	± .04
SURFACE QUALITY	100	100	100	100
FINISH	100	100	100	100
THIRD ANGLE PROJECTION	DATE	DATE	DATE	DATE
DO NOT SCALE DRAWING	DATE	DATE	DATE	DATE
REMOVE BURRS AND BREAK SHARP CORNERS	DATE	DATE	DATE	DATE
MATERIAL	DATE	DATE	DATE	DATE
SEE PARTS LIST	DATE	DATE	DATE	DATE
FINISH	DATE	DATE	DATE	DATE
NONE	DATE	DATE	DATE	DATE
TITLE		6300B MICRO VAX II WORLD BOX		
DOCUMENT NUMBER		6300B-0-DBU		
SCALE		1/2		
SHEET		1 OF 4		

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FOR MODULE
UTILIZATION
SEE SHEET 4

14
15 OR 16
OR
25

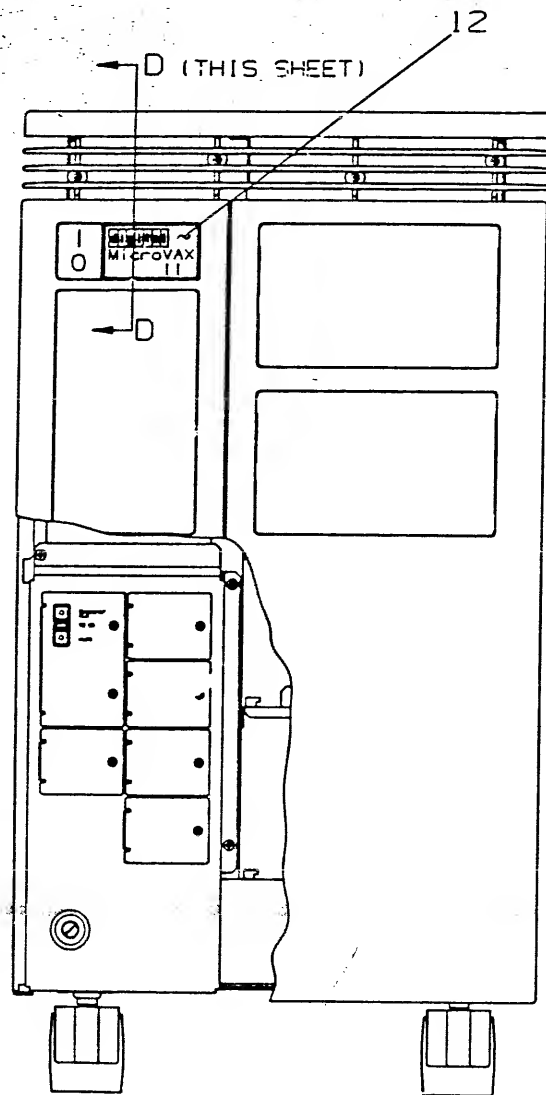
REVISIONS		
CHK	CHANGE NO	REV

TITLE		6300B MICRO VAX	SIZE CODE	D	NUMBER	6300B-0-DBU	REV	B
II WORLD BOX								
SCALE		1/2	SHEET		2	OF		4
			DIST					

PLOT AT .50

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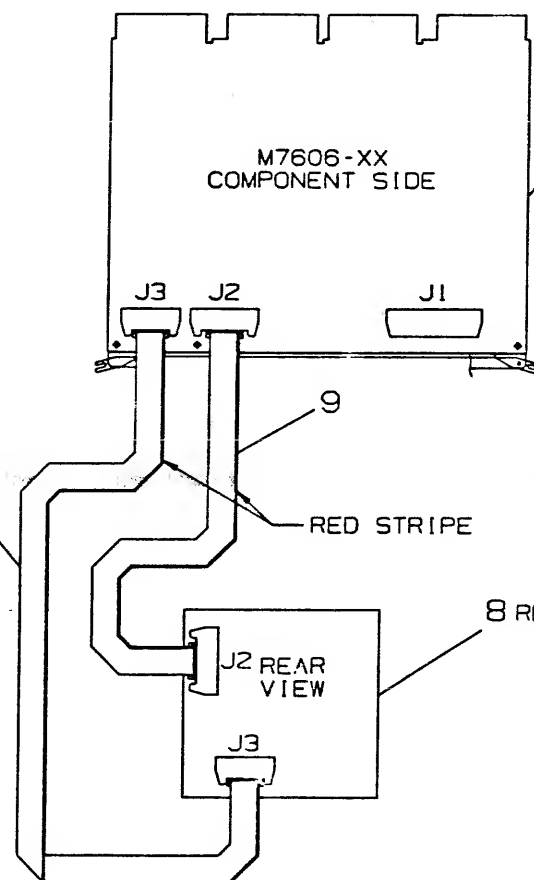
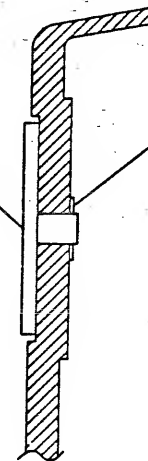
6300B-0-000E9 Vn D 2



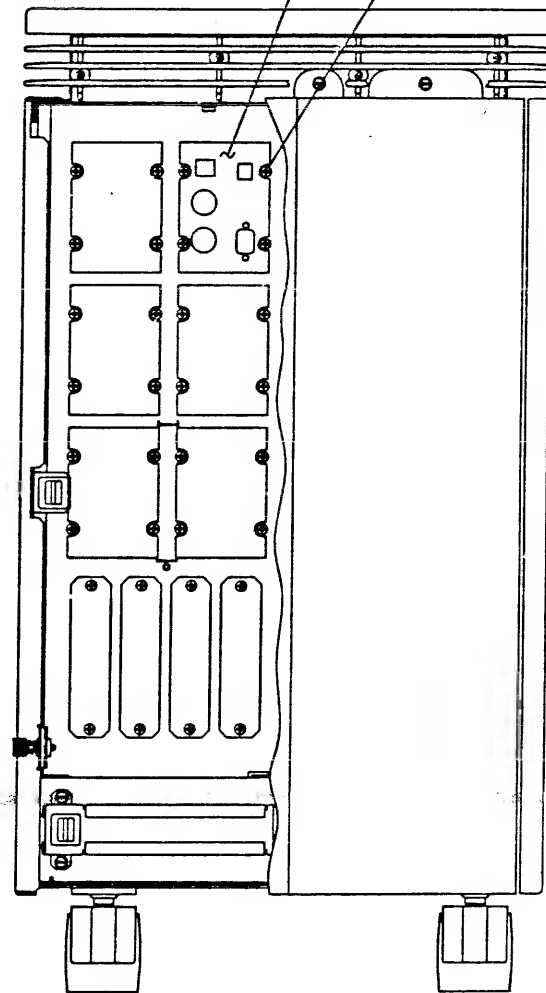
12 REF

13 (QTY 2)

SECTION D-D
SCALE 2/1



SEE DETAIL E
THIS SHEET



VIEW A-A
SEE SHT 2

VIEW B-B
SEE SHT 2

DETAIL "E"

PLOT AT .5000

REVISIONS		
CHK	CHANGE NO	REV

TITLE		6300B MICRO VAX II WORLD BOX	SIZE CODE	D UA	NUMBER	6300B-0-0BU	REV	B
SCALE		1/2	SHEET		3	OF		4

ML01

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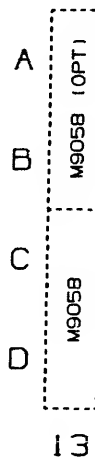
THE MODULE UTILIZATION FOR 13TH SLOT SEE NOTE 9

POSSIBLE MODULE UTILIZATIONS FOR SLOTS 5-12 ARE AS FOLLOWS (SEE NOTES 7 AND 8 THIS SHT):

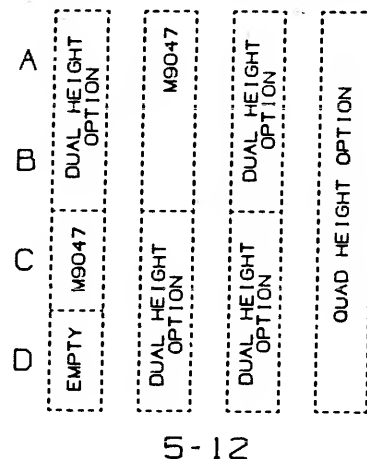
POSSIBLE MODULE UTILIZATIONS FOR SLOT 4 ARE AS FOLLOWS

POSSIBLE MODULE UTILIZATIONS FOR SLOTS 2 AND 3 ARE AS FOLLOWS (SEE NOTES 5, 6, 7 AND 8 THIS SHT):

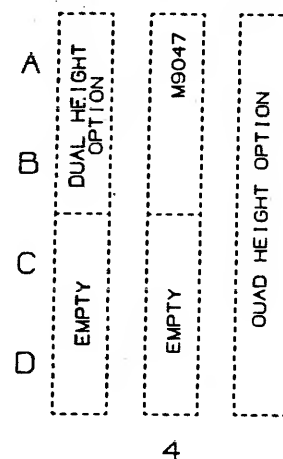
THE MODULE UTILIZATION FOR THE FIRST SLOT IS AS FOLLOWS:



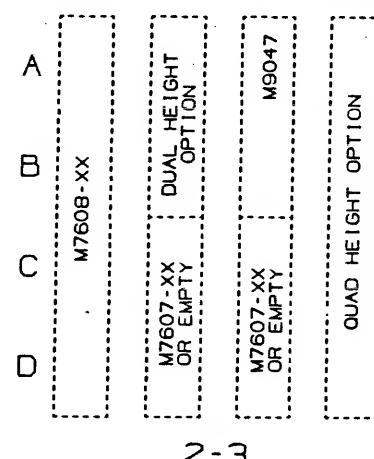
13



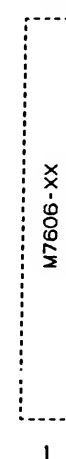
5-12



4



2-3

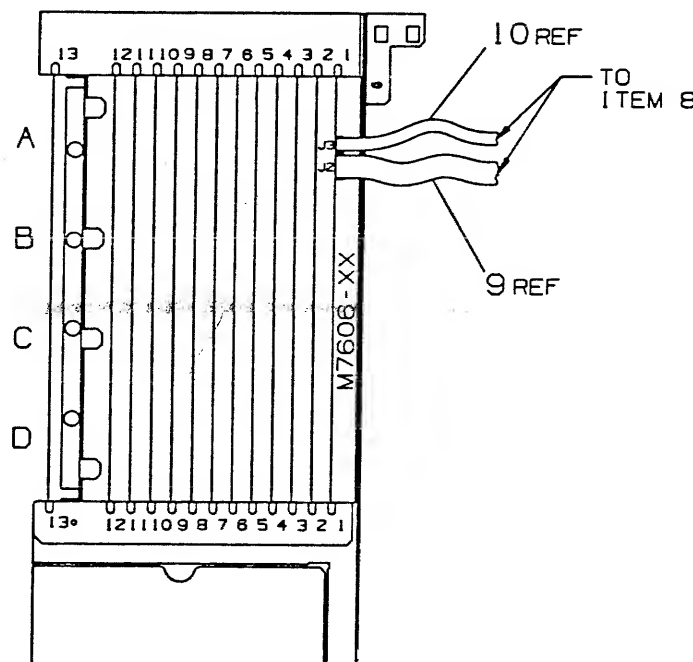


1

	12	11	10	9	8	7	6	5	4	3	2	1
XZ1	Q-BUS (19)	Q-BUS (18)	Q-BUS (17)	Q-BUS (16)	Q-BUS (15)	Q-BUS (14)	Q-BUS (13)	Q-BUS (12)	Q-BUS (11)	Q-BUS (10)	Q-BUS (9)	Q-BUS (8)
XZ2	Q-BUS (20)	Q-BUS (19)	Q-BUS (18)	Q-BUS (17)	Q-BUS (16)	Q-BUS (15)	Q-BUS (14)	Q-BUS (13)	Q-BUS (12)	Q-BUS (11)	Q-BUS (10)	Q-BUS (9)
XZ3	Q-BUS (21)	Q-BUS (20)	Q-BUS (19)	Q-BUS (18)	Q-BUS (17)	Q-BUS (16)	Q-BUS (15)	Q-BUS (14)	Q-BUS (13)	Q-BUS (12)	Q-BUS (11)	Q-BUS (10)
XZ4	Q-BUS (22)	Q-BUS (21)	Q-BUS (20)	Q-BUS (19)	Q-BUS (18)	Q-BUS (17)	Q-BUS (16)	Q-BUS (15)	Q-BUS (14)	Q-BUS (13)	Q-BUS (12)	Q-BUS (11)

SEE NOTE 4

SEE NOTES 1, 2 AND 3 THIS SHT



MODULE UTILIZATION

NOTES:

- BACKPLANE VIEWS ARE FROM THE MODULE SIDE
- THE AB ROWS OF SLOTS 1-12 AND THE CD ROWS OF SLOTS 5-12 ARE EACH LABELED "Q-BUS" BECAUSE THEY ARE INTERCONNECTED PER THE Q-BUS SPECIFICATION. THE NUMBER IN PARENTHESIS SHOWS THE PATH OF INTERRUPT AND DMA GRANT CONTINUITY; INCREASING VALUE DENOTES DECREASING PRIORITY.
- THE CD ROWS OF SLOTS 1-4 ARE LABELED "CD" BECAUSE THEY ARE CONNECTED PER THE "CD INTERCONNECT" SPECIFICATION. THIS INTERCONNECT CONNECTS SELECTED SIDE TWO PINS OF A GIVEN SLOT TO SIDE ONE PINS OF THE NEXT SLOT.
- THE BACKPLANE INCLUDES FOUR RESISTOR PACKS IN LOCATIONS XZ1, XZ2, XZ3 AND XZ4. THESE RESISTOR PACKS PROVIDE AN ADDITIONAL 120 OHMS OF TERMINATION TO THE Q-BUS LINES.
- THE SYSTEM MAY CONTAIN UP TO TWO MS630 MEMORY MODULES, LOCATED IN SLOTS 2 AND 3 (A SINGLE MS630 MODULE MUST BE LOCATED IN SLOT 2). A QUAD HEIGHT MS630 (M7608-A(X) OR M7608-B(X)) FILLS THE ENTIRE SLOT. A DUAL HEIGHT MS630 (M7607-A(X)) OCCUPIES THE CD ROWS ONLY.
- IF SLOTS 2 AND 3 (OR SLOT 3) ARE NOT USED FOR MS630 MEMORY MODULE(S), AND ARE NOT REQUIRED FOR Q-BUS OPTIONS, THEN RESERVE THEM (IT) FOR FUTURE MEMORY MODULE EXPANSION WITH M9047 GRANT CONTINUITY CARD(S) IN ROW AB.
- QUAD HEIGHT Q-BUS OPTIONS MAY BE ADDED TO ANY OPEN SLOTS, AND DUAL HEIGHT Q-BUS OPTIONS MAY BE ADDED TO ANY OPEN "Q-BUS" HALF SLOTS. ALL UNUSED "Q-BUS" HALF SLOTS WHICH PRECEED THE LAST OPTION MUST CONTAIN GRANT CONTINUITY MODULES (M9047) TO PASS GRANTS TO MODULES OF A LOWER PRIORITY. UNUSED "CD" HALF SLOTS ARE LEFT VACANT. (NOTES 2 AND 3 IDENTIFY THE "Q-BUS" AND "CD" HALF SLOTS).
- FOR MORE INFORMATION ON BACKPLANE SLOT ASSIGNMENTS, REFER TO THE SYSTEM TECHNICAL MANUAL.
- REF D-AR-7022380-0-DBU FOR MODULE UTILIZATION REQUIREMENTS.

PLOT AT .50

REVISIONS		
CHK	CHANGE NO	REV

TITLE 6300B MICRO VAX II WORLD BOX		SIZE/CONF D/UA	NUMBER 6300B-0-DBU	REV B
SCALE 1/2	SHEET 4	OF 4	DIST	

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION							
						A2	A3	B2	B3	C2	C3	D2	D3
						VARIATION REVISION LEVEL:						A2	A2
1	1	B-DD-M7606-0-0	M7606-AA		MICROVAX II W/1MB,FP,INCLUDES TI	1	1	-	-	-	-	-	-
2	2	B-DD-M7606-0-0	M7606-BA		M7606-AA W/NO FP (CPU,1MB) = M76	-	-	1	1	-	-	-	-
3	3	B-DD-M7606-0-0	M7606-CA		M7606-AA W/256KB MEM (CPU,256KB,	-	-	-	-	1	1	-	-
4	4	B-DD-M7606-0-0	M7606-DA		M7606-AA W/256KB MEM,NO FP = M76	-	-	-	-	-	-	1	1
5	5	K-PL-7022382-0-DBP	7022382-02		BA123-A ACCESSORY KIT	1	1	1	1	1	1	1	1
6	6	B-DD-7022380-0-DBU	7022380-01		BA123-A BASIC ENCLOSURE (120V)	1	-	1	-	1	-	1	-
7	7	B-DD-7022380-0-DBU	7022380-02		BA123-A BASIC ENCLOSURE (240V)	-	1	-	1	-	1	-	1
8	8	B-DD-5416744-0-0	5416744-01		FUNCTION SEL/SLU CONSOLE CONNECT	1	1	1	1	1	1	1	1
9	9	A-PS-1700712-0-0	1700712-02	A	WIRE HARN ASSY 20COND 30AWG 20SK	1	1	1	1	1	1	1	1
10	10	A-PS-1700624-0-0	1700624-01	A	CABLE ASSY,10COND,FLAT,10(2X05)I	1	1	1	1	1	1	1	1
11	11	A-PS-9010174-0-0	9010174-00	C	SCREW,SEMS PAN PHIL 6-	4	4	4	4	4	4	4	4
12	12	D-MD-7431480-0-0	7431480-03	A	MEDALLIAN SYSTEM LOGO (630QB)	1	1	1	1	1	1	1	1
13	13	A-PS-9009257-0-0	9009257-02	D	RING,RETAINER EXTERNAL FOR .188	2	2	2	2	2	2	2	2
14	14	A-PS-3617880-0-0	3617880-02		LABEL,FCC,CLASS A,PROCESSOR	1	1	1	1	1	1	1	1
15	15	A-PS-3624471-0-0	3624471-01	A	LABEL,BUSINESS COMP BA123-A2	1	-	1	-	1	-	1	-
16	16	A-PS-3624471-0-0	3624471-02	A	LABEL,BUSINESS COMP BA123-A3	-	1	-	1	-	1	-	1
17	17	A-PS-1700198-0-0	1700198-00	B	PWR CORD,TERM 3-18 250	-	REF	-	REF	-	REF	-	REF
18	18	A-PS-1700199-0-0	1700199-00	A	PWR CORD,TERM 3 250	-	REF	-	REF	-	REF	-	REF
19	19	A-PS-1700209-0-0	1700209-00	A	PWR CORD,TERM 3- .75MM 5A 250	-	REF	-	REF	-	REF	-	REF
20	20	A-PS-1700210-0-0	1700210-01	A	PWR CORD,TERM 3- .75MM 250V 6	-	REF	-	REF	-	REF	-	REF
21	21	A-PS-1700310-0-0	1700310-01	A	PWR CORD,TERM 3- .75MM 250	-	REF	-	REF	-	REF	-	REF
22	22	A-PS-1700364-0-0	1700364-01	A	PWR CORD,TERM 3- .75MM 250V	-	REF	-	REF	-	REF	-	REF
23	23	D-AR-7022380-0-DBU			BA123-A SYSTEM ARRANGEMENT	REF	REF	REF	REF	REF	REF	REF	REF
24	24	B-DD-M9047-0-0	M9047-00		QBUS GRANT CONTINUITY,1ST USED I	A/R	A/R	A/R	A/R	A/R	A/R	A/R	A/R
25	25	A-PS-3617674-0-0	3617674-22		LABEL,SERIAL/POWER,W/UL & CSA MA	A/R	A/R	A/R	A/R	A/R	A/R	A/R	A/R

REVISION HISTORY			BASIC PART NO: 630QB		DRN: D. RICHARD		DATE: 19-FEB-85		D I G I T A L				
ENG	ECO NUMBER	REV	SECTION A OF A										
UN	630QB-ML001	B	SECTION VARIATION INDEX		CHK'D: D. HEALY		DATE: 19-MAR-85		TITLE PARTS LIST				
			{A}A2,A3,B2,B3,C2,C3,D2,D3						630QB MICRO VAX II				
			{B}		DES.ENG: J. NICHOLS		DATE: 19-MAR-85		DOCUMENT NUMBER				
			{C}						SIZE CODE NUMBER REV				
			{D}		RESP.ENG.: J. NICHOLS		DATE: 19-MAR-85		K PL 630QB-0-DBP B				
			{E}		MFG.ENG.: K. WORTMAN		DATE: 19-MAR-85		RELEASE DATE: 07-MAY-85				
			{F}		ASSEMBLY NUMBER:		TOP DOCUMENT NUMBER:		FILE NAME:				
					D-UA-630QB-0-DBU		B-DD-630QB-0-DBU		ML863B.PLS				
									EDIT # 14				

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LINE ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION							
					A2	A3	B2	B3	C2	C3	D2	D3
VARIATION REVISION LEVEL:					A2	A2	A2	A2	A2	A2	A2	A2

26 NOTE: DEPENDING ON RAM VENDOR, MODULE MAY BE STAMPED AD/AH,BC/BH, CC/CH, DC/DH

D	I	G	I	T	A	L	TITLE	630QB MICRO VAX II WORLD BOX	SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
										K	PL	630QB-0-DBP	B

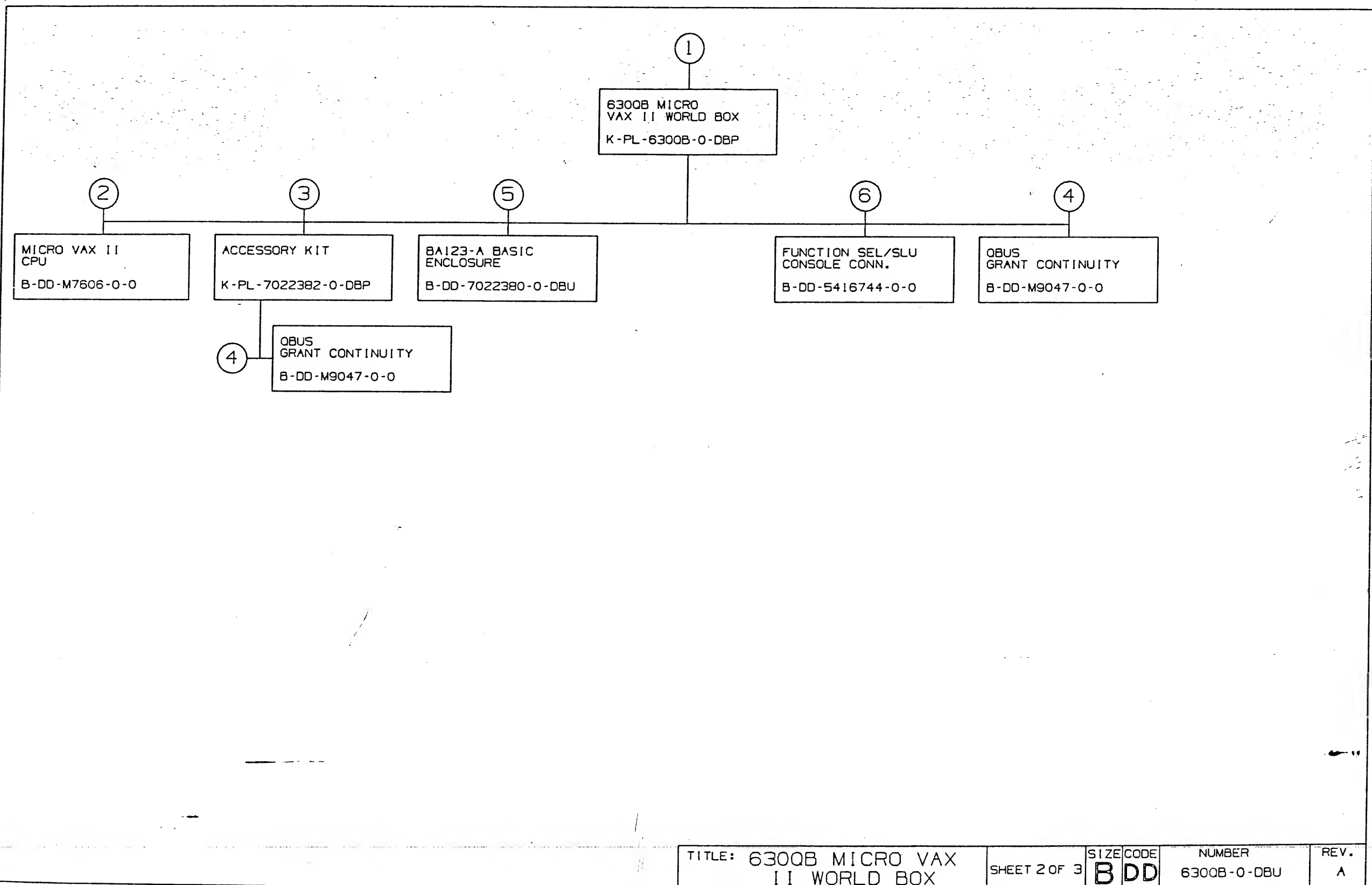
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[illegible]

FILE NAME: DD-630QB-0-DBUA

REVISIONS		CHANGE NO.	REV.	<div style="border: 1px solid black; padding: 5px;"> <div style="display: flex; justify-content: space-between;"> <div>USED ON OPTION/MODEL</div> <div> <div>DRN. D. HEALY</div> <div>DATE 25FEB85</div> </div> <div>TITLE</div> </div> <div style="text-align: center; font-size: 24px; font-weight: bold;">6300B MICRO VAX II WORLD BOX</div> <div style="display: flex; justify-content: space-between;"> <div> <div>SIZE CODE B DD</div> <div>NUMBER 6300B-0-DBU</div> </div> <div>REV A</div> </div> </div>
CHK	INITIAL	A		
SHEET 1 OF 3			<div>TOP DOC. B-DD-6300B-0-DBU</div> <div>DIST.</div>	

MLO 1



REV

NUM.BER

DD

B

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS																
		M7606	KA630	B1	C1	D1	E1	F1	H2	H2										
D-UA-M7606-0-0	1		KA630 UNIT ASSEMBLY	A	A	B	B	B	B	B										
K-PL-M7606-0-DBP	2		KA630 PARTS LIST	A	B	C	D	E	F	H										
K-PC-M7606-0-DBJ	1		P.C. DESIGN DATA BASE	E	E	E	E	E	E	E										
		5016523-01	ETCHED CIRCUIT BOARD	E1	E1	E1	E1	E1	E1	E1										
B-DD-5016523-0-0	1		DRAWING DIRECTORY	A	A	A	A	A	A	A										
B-CS-M7606-0-1	1		M7606 DRAWING DIRECTORY	-	B	B	B	B	B	B										
B-CS-M7606-0-2	1		MICROVAX II SYSTEM	-	B	B	B	B	B	B										
B-CS-M7606-0-3	1		KA630-UVAX ON Q22 BUS	-	B	B	B	B	B	B										
B-CS-M7606-0-4	1		UVAX & FPU	-	B	B	B	B	B	B										
D-CS-M7606-0-5	1		UVAX & FPU PINOUTS	-	-	-	-		A	A										
B-CS-M7606-0-6	1		ADDRESS LATCH/LOCAL MEMORY DECODE	-	B	B	B	B	B	B										
B-CS-M7606-0-7	1		MEMORY SUBSYSTEM	-	B	B	B	B	B	B										
B-CS-M7606-0-8	1		Q22 BUS INTERFACE GATE ARRAY	-	B	B	B	B	B	B										
B-CS-M7606-0-9	1		Q22 BUS INTERFACE GATE ARRAY	-	B	B	B	B	B	B										
B-CS-M7606-0-10	1		DC380 PAD ASSIGNMENT TOP VIEW LL5320 IN 144 PIN GRID ARRAY	-	B	B	B	B	B	B										
B-CS-M7606-0-11	1		REFRESH LOGIC/COUNTER	-	B	B	B	B	B	B										
B-CS-M7606-0-12	1		DIVIDE BY 12	-	B	B	B	B	B	B										
B-CS-M7606-0-13	1		SYNCHRONOUS 3 BIT COUNTER	-	B	B	B	B	B	B										
<div>NOTES:</div> <div>NOTE: MODULE PART REV H' WAS USED FOR VAXSTATION FIELD UPGRADE KIT ONLY. M7606 ECO-00006 REWORKED VARIATION M7606 AH TO EITHER M7606-ZP (NEW NEC) M7606-ZP (MITSUBIRSHI) M7606 OR M7606-ZF (HITACHI). THERE WAS NO PART REV CHANGE.</div>				REVISION HISTORY		REV.	A	B	C	D	E	F	H							
				ECO NO.	INIT	MLO01	MLO02	MLO03	MLO04	MLO05	MLO06									
				DATE	5/84	5/85	6/85	7/85	8/85	1/86	3/86									
<div>THIS DRAWING AND THE SPECIFICATIONS CONTAINED HEREIN ARE CONFIDENTIAL AND PROPRIETARY. THEY ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. THIS IS AN UNPUBLISHED WORK PROTECTED UNDER THE FEDERAL COPYRIGHT LAWS.</div> <div>1984</div>			<div>digital</div>			DRN.		D.DROZD		DATE		5/17/84		TITLE						
						CHK'D		E.LANDRY		DATE		5/17/84								
						DES. ENG.		B.MASKAS		DATE		5/17/84		DOCUMENT NUMBER						
						RESP. ENG.		B.MASKAS		DATE		5/17/84								
						MFG. ENG.		B.SCHULTE		DATE		9/24/84								SIZE
								B		DD		M7606-0-0		H						
SHEET 1 OF 4																				

DRB 128C

EN-01242-16-REVA(398)

DRAWING NO.	NO OF SHTS.	PART NO.	DESCRIPTION	REVISIONS															
B-CS-M7606-0-14	1		VECTOR HACK	-	B	B	B	B	B	B									
B-CS-M7606-0-15	1		INVERTING MUX LOGIC	-	B	B	B	B	B	B									
B-CS-M7606-0-16	1		4 to 1 MUX	-	B	B	B	B	B	B									
B-CS-M7606-0-17	1		Q-BUS SUPPORT LOGIC	-	B	B	B	B	B	B									
B-CS-M7606-0-18	1		BLK MD CTR LOGIC	-	B	B	B	B	B	B									
B-CS-M7606-0-19	1		TOGGLE FLOP	-	B	B	B	B	B	B									
B-CS-M7606-0-20	1		Q-BUS SUPPORT LOGIC	-	B	B	B	B	B	B									
B-CS-M7606-0-21	1		Q-BUS SUPPORT LOGIC	-	B	B	B	B	B	B									
B-CS-M7606-0-22	1		Q-BUS SUPPORT LOGIC	-	B	B	B	B	B	B									
B-CS-M7606-0-23	1		Q-BUS SUPPORT LOGIC	-	B	B	B	B	B	B									
B-CS-M7606-0-24	1		POWER BUFFER MACRO	-	B	B	B	B	B	B									
B-CS-M7606-0-25	1		BIDIRECT BUFFER	-	B	B	B	B	B	B									
B-CS-M7606-0-26	1		MUX LOGIC	-	B	B	B	B	B	B									
B-CS-M7606-0-27	1		TRANSLATION MAP GROUP	-	B	B	B	B	B	B									
B-CS-M7606-0-28	1		KA630 Q-BUS INTERFACE	-	B	B	B	B	B	B									
B-CS-M7606-0-29	1		UVAX INTERFACE GATE ARRAY	-	B	B	B	B	B	B									
B-CS-M7606-0-30	1		DC379 PAD ASSIGNMENT TOP VIEW LL5320 IN 144 PIN GRIP ARRAY	-	B	B	B	B	B	B									
B-CS-M7606-0-31	1		UVAX INTERFACE GATE ARRAY DATA PATH		B	B	B	B	B	B									
B-CS-M7606-0-32	1		UVDAL I/O BUFFERS, ADDR LATCHES	-	B	B	B	B	B	B									

NOTES:	REVISION HISTORY		
	DATE	ECO NO.	REV.
	5/84	INIT	A
	5/85	ML001	B
	6/85	ML002	C
	7/85	ML003	D
	8/85	ML004	E
	1/86	ML005	F
	3/86	ML006	H

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1984

digital

DRN. D.DROZD

CHK'D E.LANDRY

DES. ENG. B.MASKAS

RESP. ENG. B.MASKAS

MFG. ENG. B.SCHULTE

DATE 5/17/84

DATE 5/17/84

DATE 5/17/84

DATE 5/17/84

DATE 9/24/84

TITLE

KA630

DOCUMENT NUMBER

SIZE B

CODE DD

NUMBER M7606-0-0

REV. H

SHEET 2 OF 4

DRAWING NO.	NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS																	
B-CS-M7606-0-33	1		ADDRESS DECODER	-	B	B	B	B	B	B											
B-CS-M7606-0-34	1		EXCEPTIONS AND INTERRUPTS	-	B	B	B	B	B	B											
B-CS-M7606-0-35	1		UVAX INPUTS AND I/O PINS	-	B	B	B	B	B	B											
B-CS-M7606-0-36	1		BOOT/DIAG REG., MEM ERR ADDR REG.	-	B	B	B	B	B	B											
B-CS-M7606-0-37	1		EPR BUS, X DAL BUS	-	B	B	B	B	B	B											
B-CS-M7606-0-38	1		INTERNAL DATA BUSES	-	B	B	B	B	B	B											
B-CS-M7606-0-39	1		MISC. CONTROL STROBES	-	B	B	B	B	B	B											
B-CS-M7606-0-40	1		RESET COUNTER, POWER UP/DOWN CNTRL	-	B	B	B	B	B	B											
B-CS-M7606-0-41	1		MEMORY SYSTEM ERROR REGISTER	-	B	B	B	B	B	B											
B-CS-M7606-0-42	1		TIME OF YEAR (TOY) CLOCK	-	B	B	B	B	B	B											
B-CS-M7606-0-43	1		CONSOLE SERIAL LINE INTERFACE	-	B	B	B	B	B	B											
B-CS-M7606-0-44	1		LEDS AND CONFIGURATION CONNECTOR	-	B	B	B	B	B	B											
B-CS-M7606-0-45	1		DECOUPLING CAPACITORS	-	B	B	B	B	B	B											
B-CS-M7606-0-46	1		KA630 STATE MACHINES	-	B	B	B	B	B	B											
B-CS-M7606-0-47	1		UVAX CYCLE CONTROLLER	-	B	B	B	B	B	B											
B-CS-M7606-0-48	1		MEMORY SEQUENCER	-	B	B	B	B	B	B											
B-CS-M7606-0-49	1		MEMORY SEQUENCER SUPPORT	-	B	B	B	B	B	B											
B-CS-M7606-0-50	1		Q22 BUS STATE MACHINES	-	B	B	B	B	B	B											
D-CS-M7606-0-51	1		KA630 MEMORY ARBITER LISTING	-	-	-	-	-	A	A											
NOTES:				REVISION HISTORY	REV.	A	B	C	D	E	F	H									
					ECO NO.	INIT	MLO01	MLO02	MLO03	MLO04	MLO05	MLO06									
					DATE	5/84	5/85	6/85	7/85	8/85	1/86	3/86									
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										D.DROZD		5/17/84									
										CHK'D		DATE									
										E.LANDRY		5/17/84									
										DES. ENG.		DATE									
										B.MASKAS		5/17/84									
				RESP. ENG.		DATE		SIZE		CODE		NUMBER		REV							
				B.MASKAS		5/17/84		B		DD		M7606-0-0		H							
				MFG. ENG.		DATE															
				B.SCHULTE		9/24/84															
														SHEET 3 OF 4							

H REV										0-0-9097M NUMBER										DD CODE		B SIZE	
DRAWING NO.		NO. OF SHTS.	PART NO.	DESCRIPTION	REVISIONS																		
B-CS-M7606-0-52		1		KA630 MEMORY SYSTEM ARBITER STATE FLOW DIAGRAMS	-	B	B	B	B	B	B												
B-CS-M7606-0-53		1		KA630 MEMORY SYSTEM ARBITER STATE FLOW DIAGRAMS	-	B	B	B	B	B	B												
D-CS-M7606-0-54		1		KA630 LOCAL I/O CONTROL MACHINE	-	-	-	-	-	A	A												
				UL TESTING	-	-	-	-	-														
B-CS-M7606-0-55		1		KA630 LOCAL I/O BUS CONTROL	-	B	B	B	B	B	B												
D-CS-M7606-0-56		1		KA630 Q-BUS ARBITRATION CONTROL MACHINE LISTING	-	-	-	-	-	A	A												
B-CS-M7606-0-57		1		Q-BUS ARBITRATION CONTROLLER DETAILED CONTROL FLOW DIAGRAM	-	B	B	B	B	B	B												
D-CS-M7606-0-58		1		Q22 BUS MASTER CONTROL MACHINE LISTING	-	-	-	-	-	A	A												
B-CS-M7606-0-59		1		Q22 BUS MASTER CONTROL MACHINE FLOW DIAGRAM	-	B	B	B	B	B	B												
D-CS-M7606-0-60		1		Q22 BUS SLAVE CONTROL MACHINE LISTING	-	-	-	-	-	A	A												
B-CS-M7606-0-61		1		Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM	-	B	B	B	B	B	B												
B-CS-M7606-0-62		1		Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM	-	B	B	B	B	B	B												
D-CS-M7606-0-63		1		IKKL RAS DECODE FROM (ETS) LISTING	-	-	-	-	-	A	A												
D-CS-M7606-0-64		1		PALASM LISTING FOR PALISLSA DEVICES	-	-	-	-	-	A	A												
D-CS-M7606-0-65		1		MNEMONIC DICTORY	-	-	-	-	-	A	A												
K-DO-M7606-0-0		24		M7606 CROSS REF LIST	-	A	A	A	A	A	A												
NOTES:					REVISION HISTORY	REV.	A	B	C	D	E	F	H										
						ECO NO.	INIT	MLO01	MLO02	MLO03	MLO04	MLO05	MLO06										
						DATE	5/84	5/85	6/85	7/85	8/85	1/86	3/86										
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										CHK'D E.LANDRY		DATE 5/17/84											
										DES. ENG. B.MASKAS		DATE 5/17/84		DOCUMENT NUMBER M7606-0-0									
										RESP. ENG. B.MASKAS		DATE 5/17/84											
										MFG. ENG. B.SCHULTE		DATE 9/24/84								SIZE B		CODE DD	
												SHEET		4 OF		4							

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REWORK INSTRUCTIONS

1. COMPONENT DELETES

2-1 DELETE E21 P/N 23035E6-00

2-2 DELETE E22 P/N 23034E6-CO

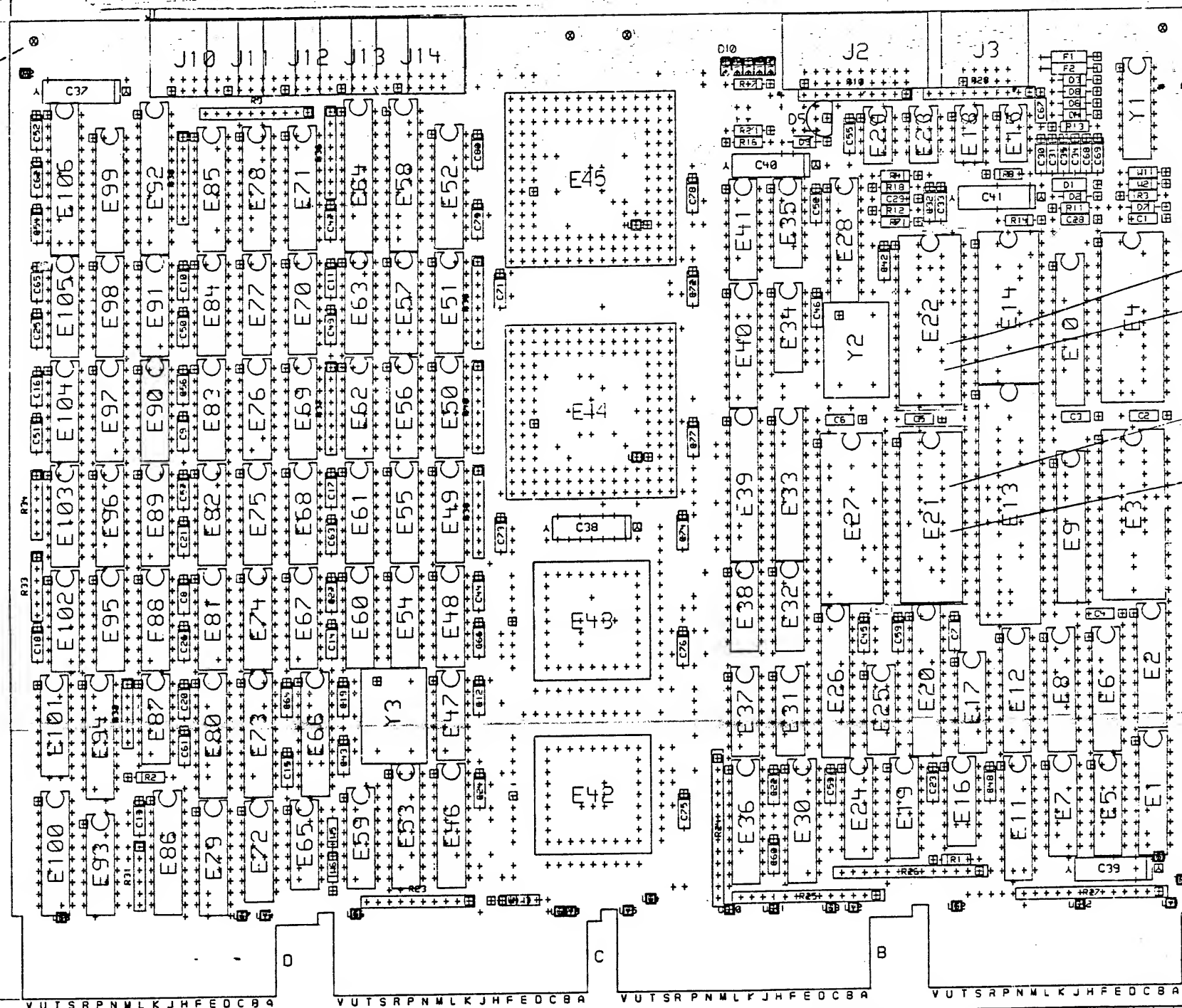
2. COMPONENT AIDS.

2-3 DELETE E21 P/N 23063E6-00

2-4 DELETE E22 P/N 23062E6-00

94-
(QTY. 4)

COMPONENT SIDE VIEW



NOTES: 1. NOT INSTALLED

STEP E	↑ Y AXIS _____ STEP ____ TIMES
REPEAT	→ X AXIS _____ STEP ____ TIMES

CHK	CHANGE NO	REV
M7606-MLOO	B	

ETCH REV. 31

SIGNATURES		DATE		digital			
CRN.							
CHK'D.							
MECH. ENG.				TITLE			
PROJ. ENG.				A-B-C-D			
PROD. WITH				SIZE		NUMBER	
SCALE				0		UAM 7606	
SHT.		GF					
NEXT HIGHER ASS.							

MS# 25

KA630-AA,-AB,-AC,-AD (M7606) DRAWING DIRECTORY

DATA PATH

0 MICROVAX II SYSTEM

1 KA630 - uVAX on Q22 Bus

1.1 uVAX & FPU

1.1.1 uVAX & FPU PINOUTS

1.2 ADDRESS LATCH/LOCAL MEMORY DECODE

1.3 Memory Subsystem

1.4 Q22 Bus Interface Gate Array

1.4.1-1.4.2, 1.4.1.1-1.4.1.9

1.5 Translation Map Group

1.6 KA630 QBUS INTERFACE

1.7 uVAX Interface Gate Array

1.7.1-1.7.2, 1.7.2.1-1.7.2.10

1.8 TOY CLOCK

1.9 Console Serial Line Interface

1.10 LEDS and Configuration Connector

1.11 Decoupling Capacitors

CONTROL

2 KA630 State Machines

2.1 uVAX Cycle Controller

2.1.1 MEMORY SEQUENCER

2.1.2 MEMORY SEQUENCER SUPPORT

2.2 Q22 BUS STATE MACHINES

MISC.

3 KA630 MEMORY ARBITER LISTING

3.1-3.2 KA630 MEMORY ARBITER FLOW DIAGRAM

4 KA630 LOCAL I/O CONTROL MACHINE LISTING

4.1 KA630 LOCAL I/O CONTROL MACHINE FLOW DIAGRAM

5 Q22 BUS ARBITRATION CONTROL MACHINE LISTING

5.1 Q22 BUS ARBITRATION CONTROL MACHINE FLOW DIAGRAM

6 Q22 BUS MASTER CONTROL MACHINE LISTING

6.1 Q22 BUS MASTER CONTROL MACHINE FLOW DIAGRAM

7 Q22 BUS SLAVE CONTROL MACHINE LISTING

7.1-7.2 Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM

8 1KX4 RAS DECODE PROM (E79) LISTING

9 PALASM LISTINGS FOR PAL16L8A DEVICES

10 MNEMONIC DICTIONARY

DRAWING

TITLE=DIRECTORY

ABBREV=DIRECT

CIRCUIT+TYPE=DOCUMENTATION

LAST+MODIFIED=Sun Dec 9 16:50:34 1984

DEFINE

X+FIRST=0

X+STEP=SIZE

REVISION	1	JOE MULLIN
CHK	CHANGE NO	REV
DATE	12/09/84	11:55
BY	JOE MULLIN	

digital

DATE ENG. 12/09/84
DATE BOARD LOCATION: 12/09/84
DATE BOARD LOCATION: 12/09/84

TITLE: M7606 DRAWING DIRECTORY

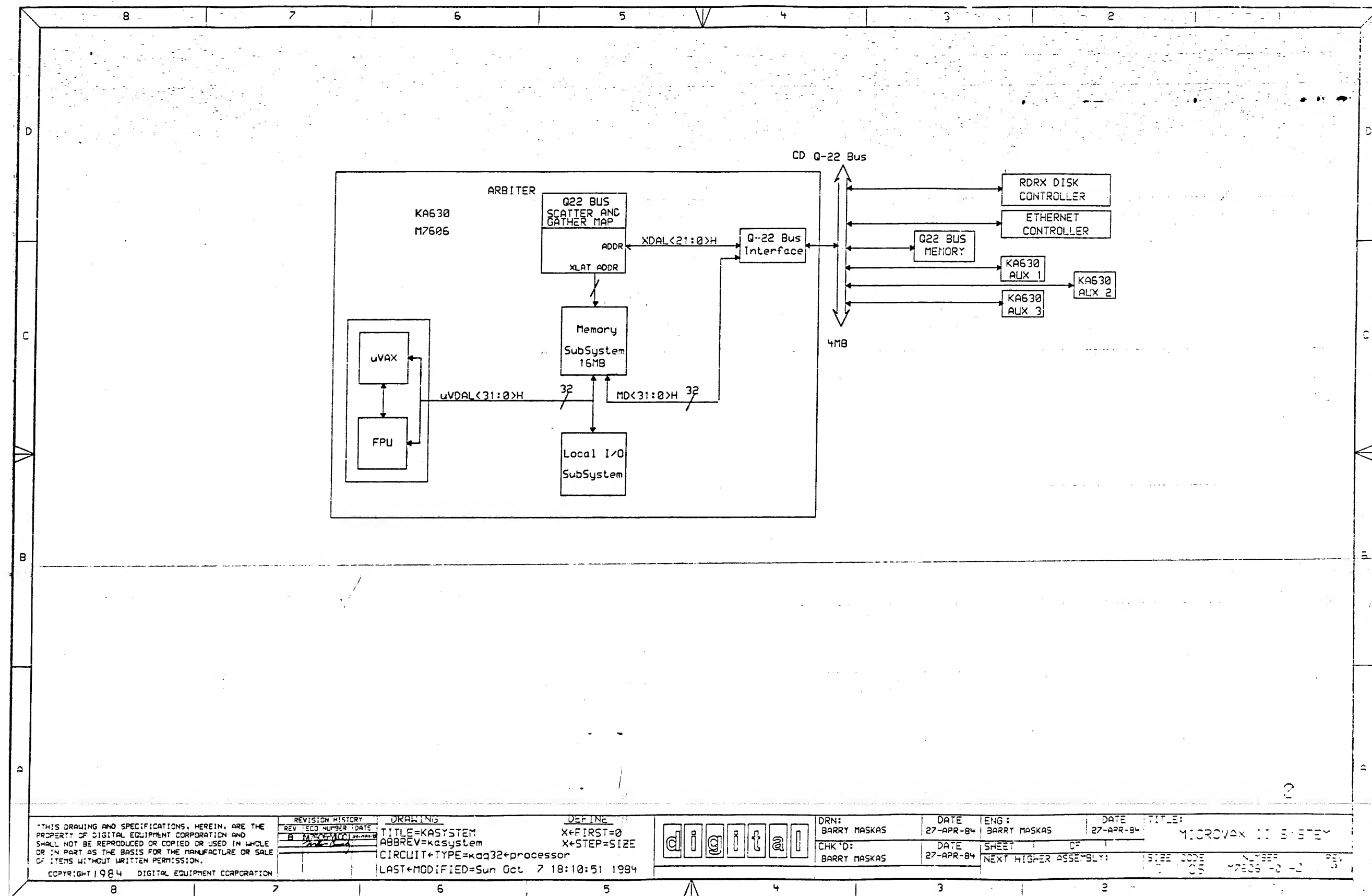
USRA: FIRST USED ON OPTION/MODEL:

TOP DOCUMENT NUMBER:

SIZE CODE: 2:CS

NUMBER: M7606-0-1

3



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REVISION HISTORY		
REV	ECO NUMBER	DATE
1	1	27-APR-84

DRAWING

TITLE=KASYSYSTEM

ABBREV=kasystem

CIRCUIT+TYPE=kag32+processor

LAST+MODIFIED=Sun Oct 7 18:10:51 1984

DEFINE

X+FIRST=0

X+STEP=SIZE

digital

DRN: BARRY MASKAS

CHK'D: BARRY MASKAS

DATE 27-APR-84

DATE 27-APR-84

ENG: BARRY MASKAS

SHEET 1 OF 1

NEXT HIGHER ASSEMBLY:

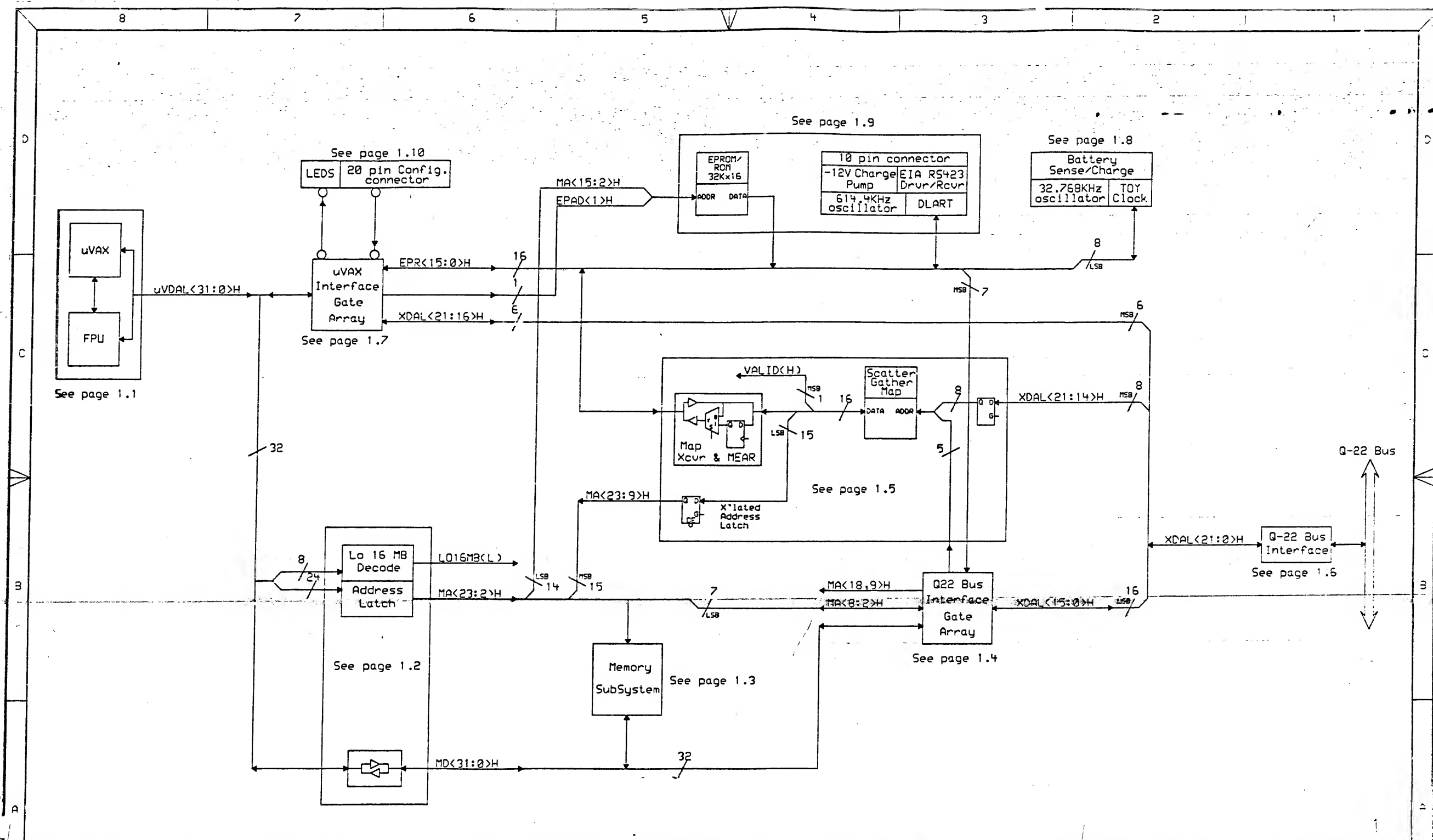
DATE 27-APR-84

TITLE: MICROVAX II SYSTEM

SIZE CODE

NUMBER

REV



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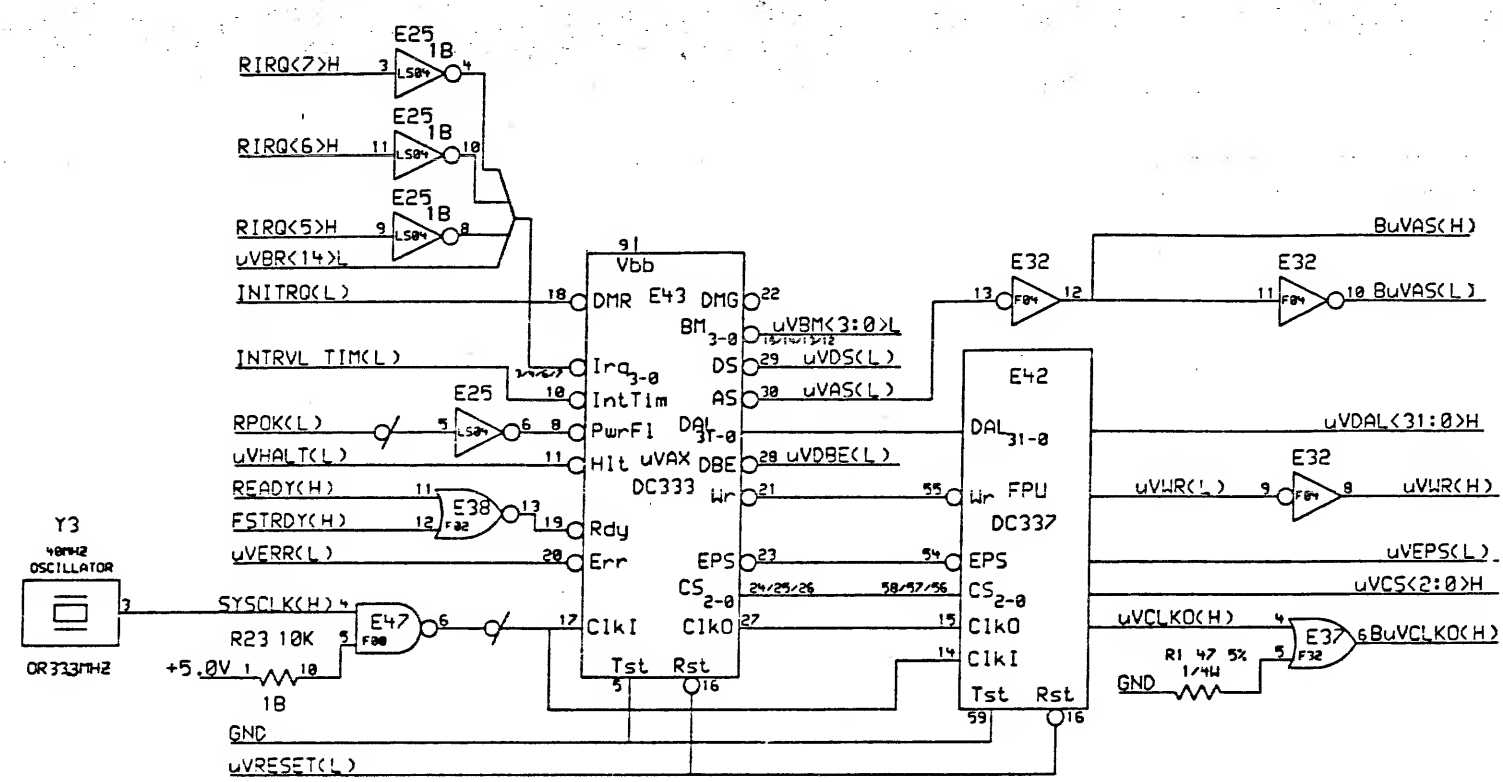
REVISION HISTORY		
REV	TECO NUMBER	DATE
1	1	10/12/84

DRAWING
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 ABBREV=kda32
 CIRCUIT+TYPE=kda32+processor
 LAST*MODIFIED=Fri Oct 12 11:27:57 1984

DEFINE
 X*FIRST=0
 X*STEP=SIZE
 digital

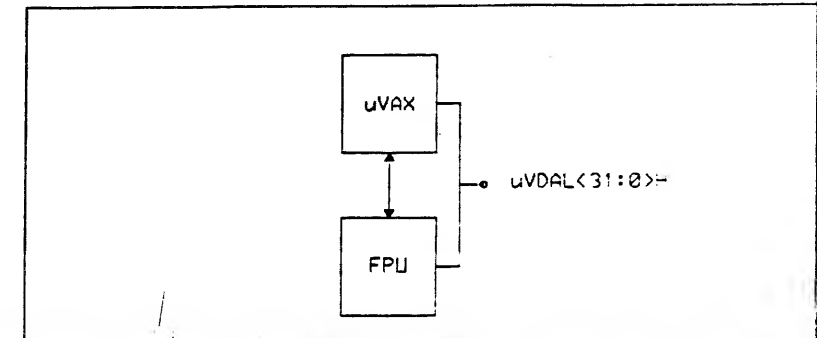
DRN: R. McNamara	DATE 3-OCT-84	ENG: R. McNamara	DATE 3-OCT-84
CHK'D: R. McNamara	DATE 3-OCT-84	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:

TITLE: KA630 - uVAX on Q22 Bus			
SIZE C	CODE CS	NUMBER M7605 -2 -3	REV 1



uVAS<L> CYCLES
uVCS<2:0>H uVWR<L>
LHH H interrupt acknowledge (IAK)
HLL H read (1 - stream)
HLH H read (lock)
HLL H read (0 - stream)
HLH H write (unlock)
HLL H write (0 - stream)
x => don't care

uVEPS<L> CYCLES
uVCS<2:0>H uVWR<L>
HLH H read data
HLL H read response (uVCS<2> pulled low by responder)
HLH H write command (fpu)
HLL H write data
HLL H write command (non-fpu)



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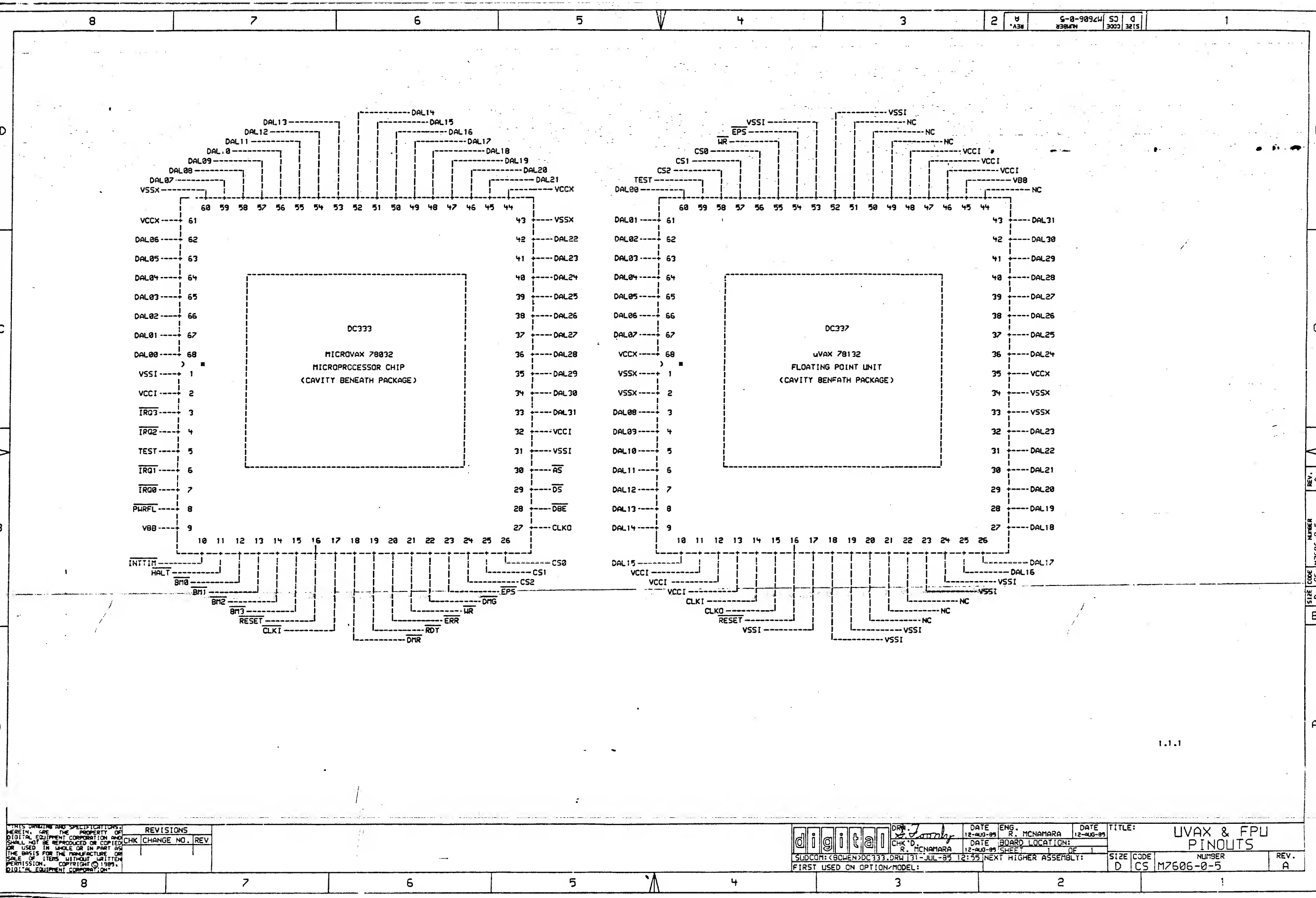
REVISION HISTORY		
REV	ECO NUMBER	DATE
1	1	3-10-84

DRAWING
TITLE=UVAX
ABBREV=UVAX+FPU
CIRCUIT+TYPE=UVAX/FPU
LAST*MODIFIED=Fri Nov 9 18:39:57 1984

DEFINE
X*FIRST=0
X*STEP=SIZE
digital

DRN: BARRY MASKAS	DATE 3-OCT-84	ENG: BARRY MASKAS	DATE 3-OCT-84
CHK'D: BARRY MASKAS	DATE 3-OCT-84	SHEET 1 OF 1	
		NEXT HIGHER ASSEMBLY:	

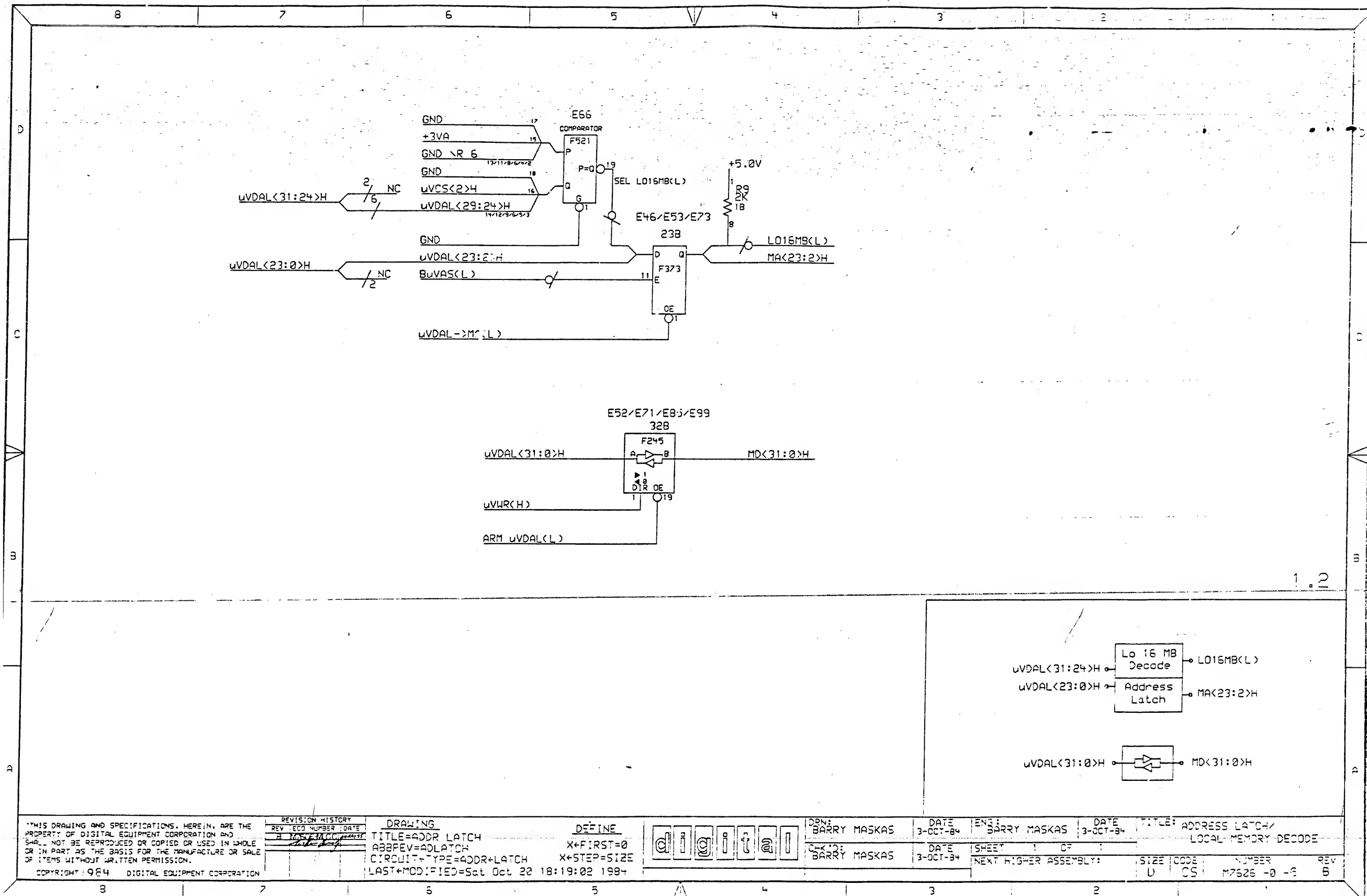
TITLE: UVAX & FPU
SIZE CODE NUMBER
D 105 17526 -2 -1 B



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REVISIONS		
CHK	CHANGE NO.	REV

digital	DATE 12-AUG-89	ENG. R. MCNAMARA	DATE 12-AUG-89	TITLE: UVAX & FPU PINOUTS
	CHK'D R. MCNAMARA	DATE 12-AUG-89	SHEET 1 OF 1	BOARD LOCATION:
SUDCOM: (BOWEN)DC333.DRW 131-JUL-85 12:55				NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL:				
SIZE D	CODE CS	NUMBER M7606-0-5	REV. A	



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REVISION HISTORY
REV ECD NUMBER DATE
H M7526-00-00

DRAWING
TITLE=ADDR LATCH
ABBREV=ADLATCH
CIRCUIT TYPE=ADDR+LATCH
LAST MODIFIED=Sat Oct 20 18:19:02 1984
DEFINE
X*FIRST=0
X*STEP=SIZE

digital

DRN: BARRY MASKAS
DATE 3-OCT-84
ENR: BARRY MASKAS
DATE 3-OCT-84
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

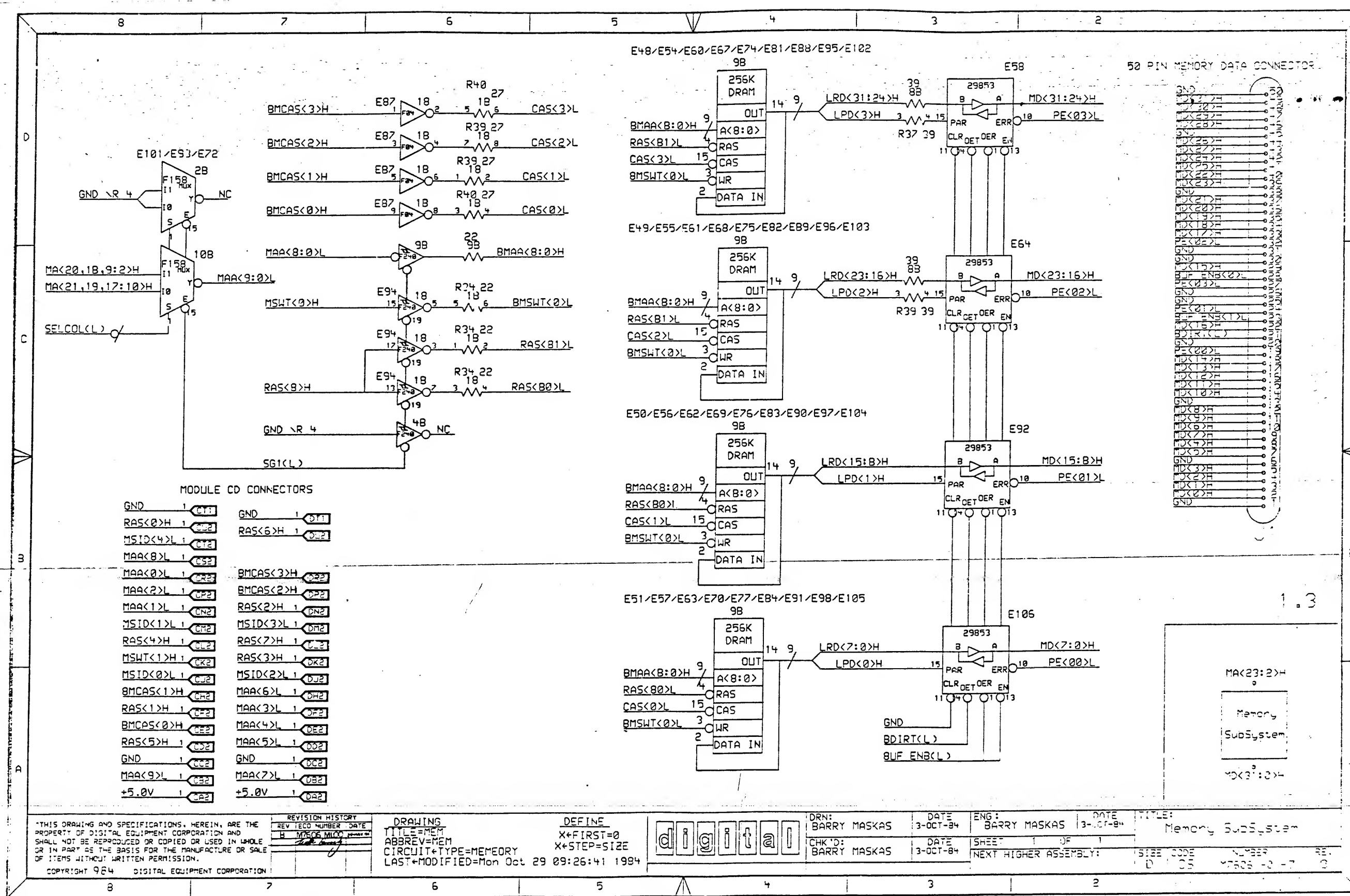
DATE 3-OCT-84

DATE 3-OCT-84

DATE 3-OCT-84

TITLE: ADDRESS LATCH/
LOCAL MEMORY DECODE

SIZE CODE NUMBER REV
U CS M7526 -0 -6 B



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REVISION HISTORY		
REV	TECO NUMBER	DATE
1	MEMO5 M100	10/29/84

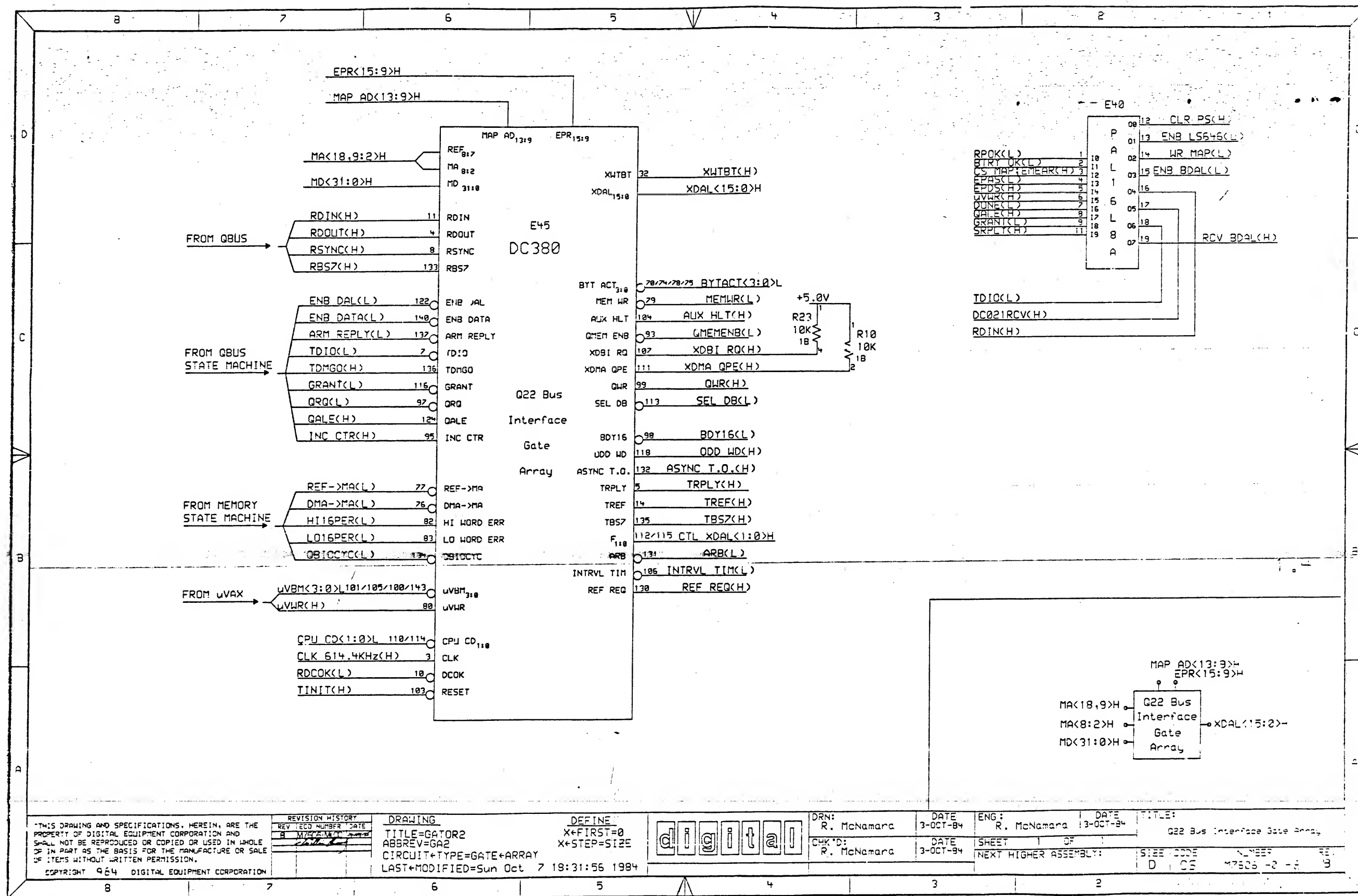
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ABBREV=MEM
CIRCUIT+TYPE=MEMEORY
LAST+MODIFIED=Mon Oct 29 09:26:41 1984

DEFINE
X+FIRST=0
X+STEP=SIZE



DRN: BARRY MASKAS	DATE: 3-OCT-84	ENG: BARRY MASKAS	DATE: 3-OCT-84
CHK'D: BARRY MASKAS	DATE: 3-OCT-84	SHEET 1 OF 1	
		NEXT HIGHER ASSEMBLY:	

TITLE: Memory Subsystem		SIZE CODE	NUMBER	RE.
		D 105	7505-2-7	2



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REVISION HISTORY	
REV	DATE
1	10/7/84

DRAWING
 TITLE=GATOR2
 ABBREV=GA2
 CIRCUIT TYPE=GATE+ARRAY
 LAST MODIFIED=Sun Oct 7 18:31:56 1984

DEFINE
 X*FIRST=0
 X*STEP=SIZE

digital

DRN:
R. McNamara

DATE
3-OCT-84

ENG:
R. McNamara

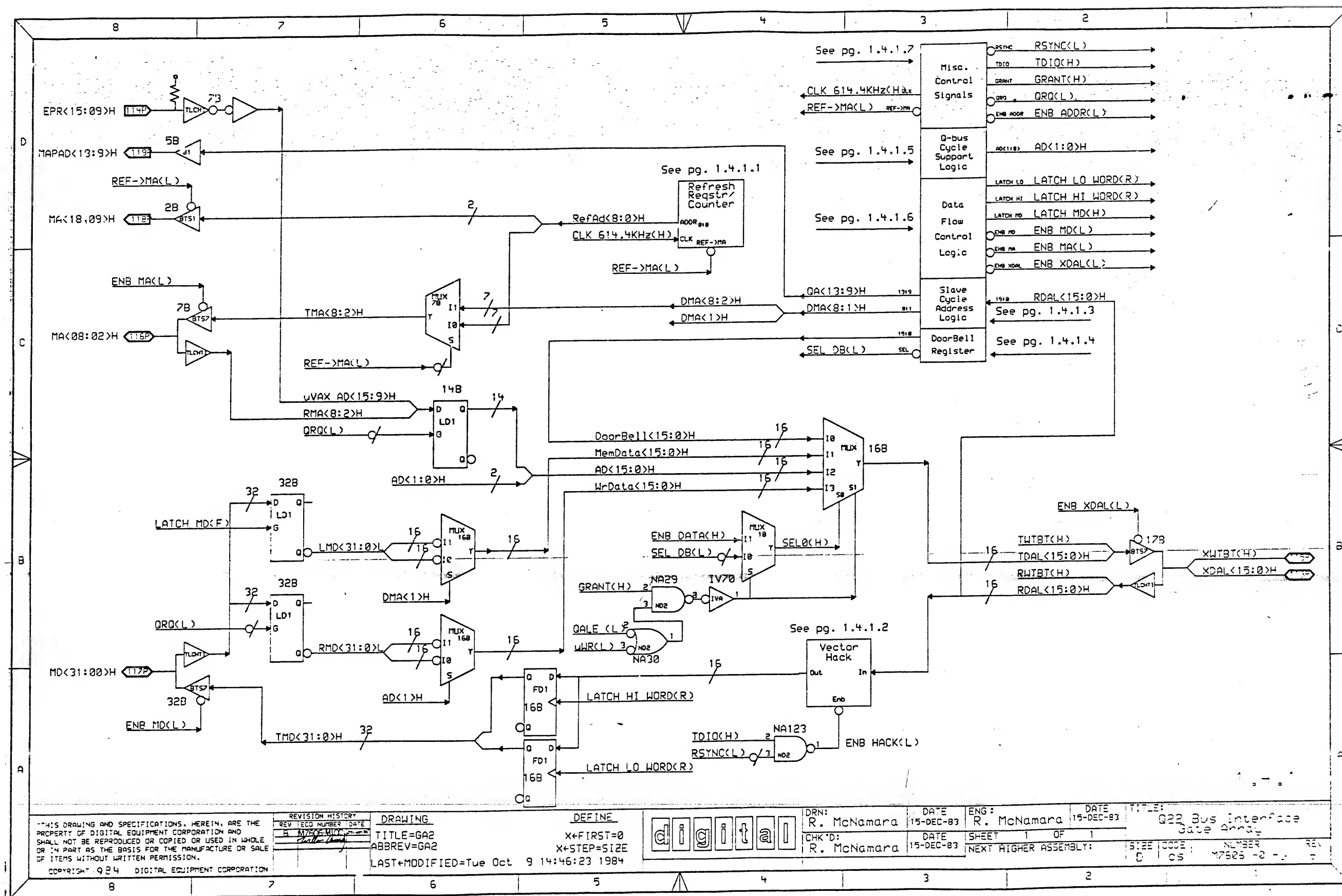
DATE
3-OCT-84

SHEET 1 OF 1

NEXT HIGHER ASSEMBLY:

TITLE:
G22 Bus Interface Gate Array

SIZE CODE
D 105 47505 -2 -3 3



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REV	ECO	NUMBER	DATE
1		1	15-DEC-83

DRAWING
 TITLE=GA2
 ABBREV=GA2
 LAST MODIFIED=Tue Oct 9 14:46:23 1984

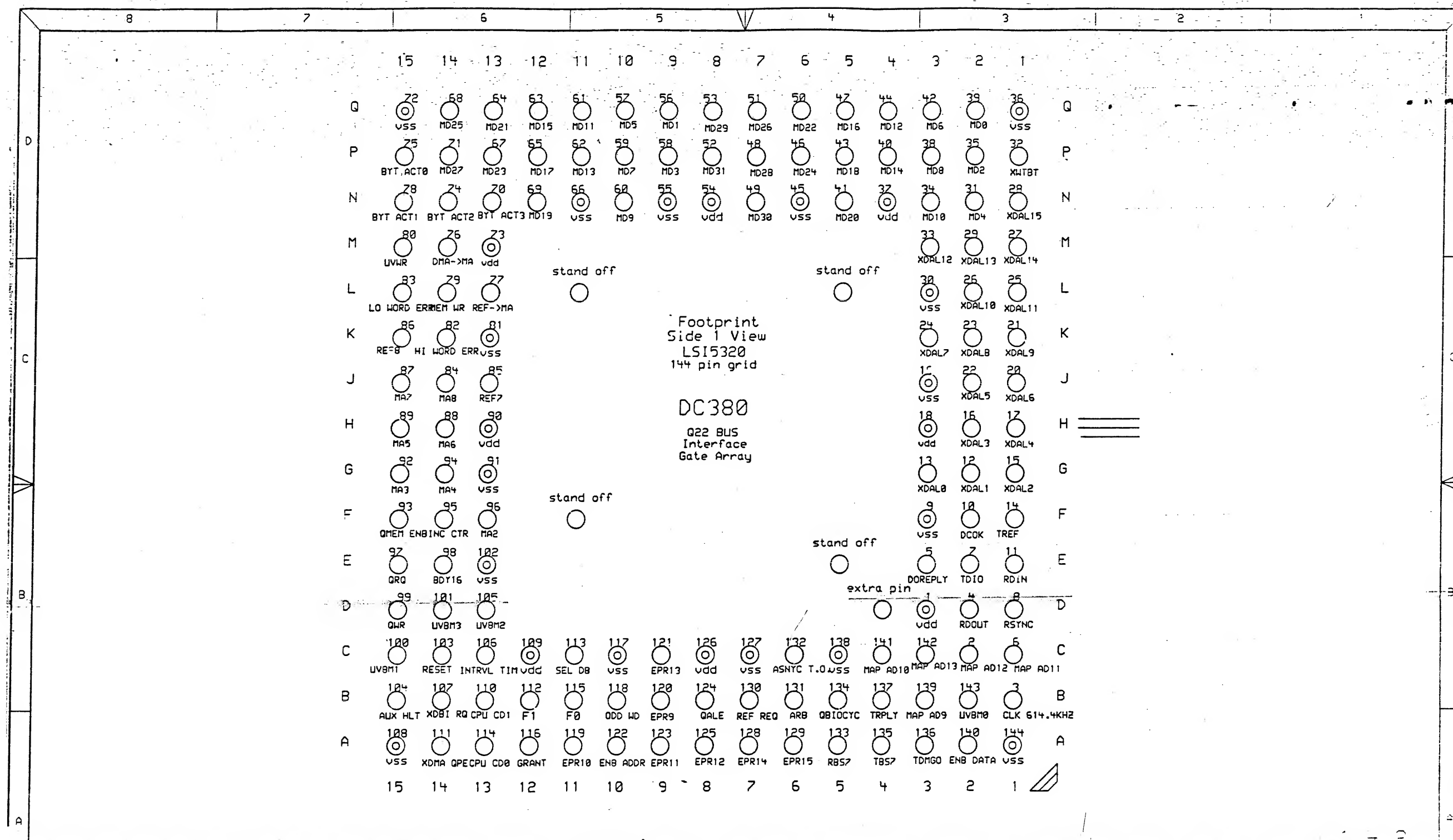
DEFINE
 X+FIRST=0
 X+STEP=SIZE

digital

DRN: R. McNamara
 DATE 15-DEC-83
 CHK'D: R. McNamara
 DATE 15-DEC-83

ENG: R. McNamara
 DATE 15-DEC-83
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE: Q22 Bus Interface Gate Array
 SIZE CODE NUMBER
 0 cs 17605 -2 -



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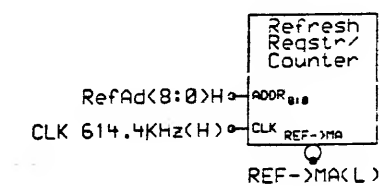
REVISION HISTORY		
REV	ECO NUMBER	DATE
1	1	10-1-84

digitai

DRN: R. McNamara
CHK'D: R. McNamara
DATE: 18-MAY-84

ENG: R. McNamara
SHEET: 1 OF 1
DATE: 18-MAY-84
NEXT HIGHER ASSEMBLY:

TITLE: DC380 PAD ASSIGNMENT TOP VIEW
LS15320 IN 144 PIN GRID ARRAY
SIZE CODE: M7625 -0 -10
NUMBER: 3



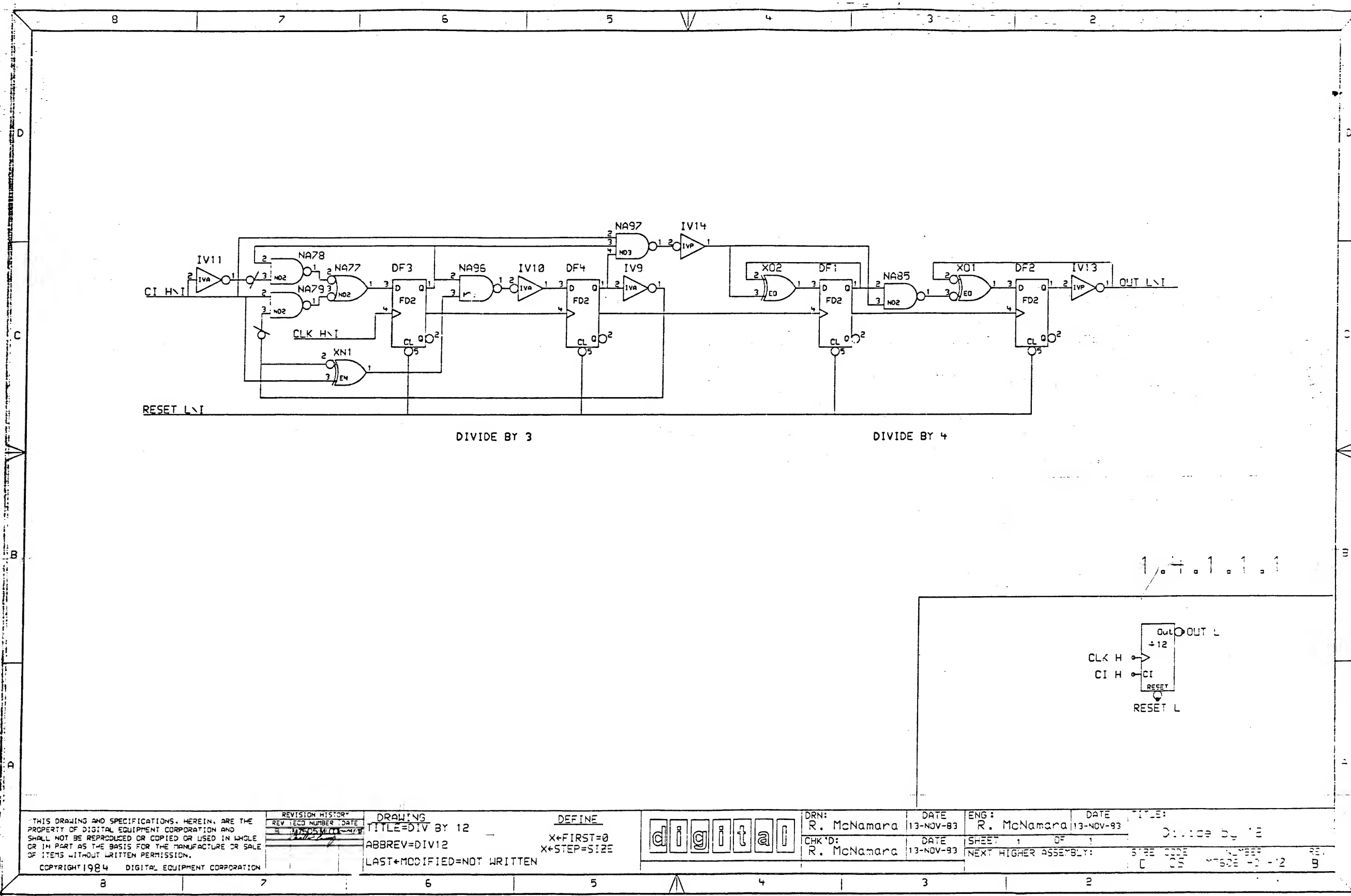
COPYRIGHT 1964 DIGITAL EQUIPMENT CORPORATION

В 31.06.10. 42/10
2010-2011

LAST MODIFIED=Wed Oct 10 19:06:07 1984

SIZE	CODE	NUMBER	REV
------	------	--------	-----

SIZE	CODE	NUMBER	REV
0	CS	M7625 -0 -11	B



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REVISION HISTORY		
REV	DESCRIPTION	DATE
1	INITIAL DESIGN	11/13/93

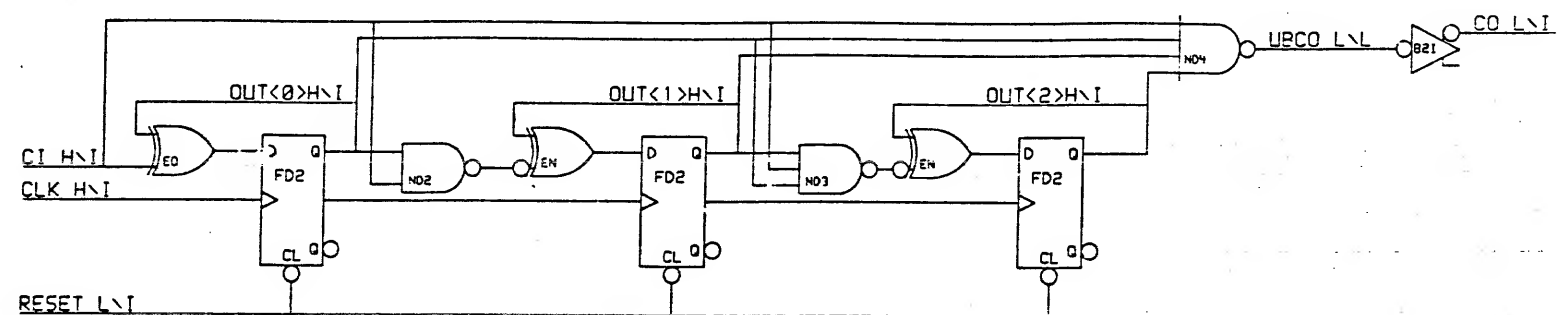
DRAWING
TITLE=DIV BY 12
ABBREV=DIV12
LAST MODIFIED=NOT WRITTEN
X*FIRST=0
X*STEP=SIZE

digital

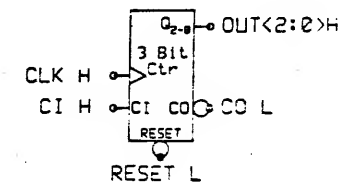
DRN: R. McNamara
CHK'D: R. McNamara
DATE: 13-NOV-93

ENG: R. McNamara
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

DATE: 13-NOV-93
TITLE: Divide by 12
SIZE: 11x17
NO. OF SHEETS: 1
REV: 0



1.4.1.1.2



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REVISION HISTORY		
REV	ECO NUMBER	DATE
1	17805	10/20/84

DRAWING
 TITLE=3 BIT CTR
 ABBREV=3BCTR
 CIRCUIT+TYPE=3BITCTR
 LAST+MODIFIED=Sat Oct 20 18:47:47 1984

DEFINE
 X+FIRST=0
 X+STEP=SIZE

DRN:
 R. McNamara
 CHK'D:
 R. McNamara

DATE
 6-NOV-83
 DATE
 6-NOV-83

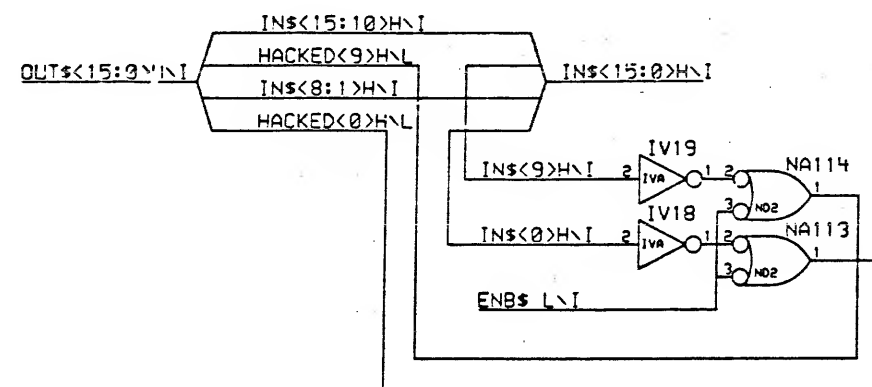
ENG:
 R. McNamara
 SHEET
 1 OF 1

DATE
 6-NOV-83
 NEXT HIGHER ASSEMBLY:

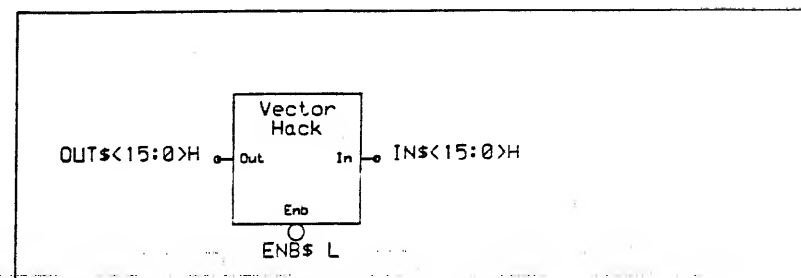
TITLE:
 Synchronous 3 Bit Counter

SIZE CODE
 D 05

REVISION
 1-3



1.4.1.2



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REV	ECO	NUMBER	DATE
1		1	10/10/84

DRAWING
TITLE=VECTOR HACK
ABBREV=VCTRCK
LAST*MODIFIED=Wed Oct 10 19:16:55 1984

DEFINE
X*FIRST=0
X*STEP=SIZE

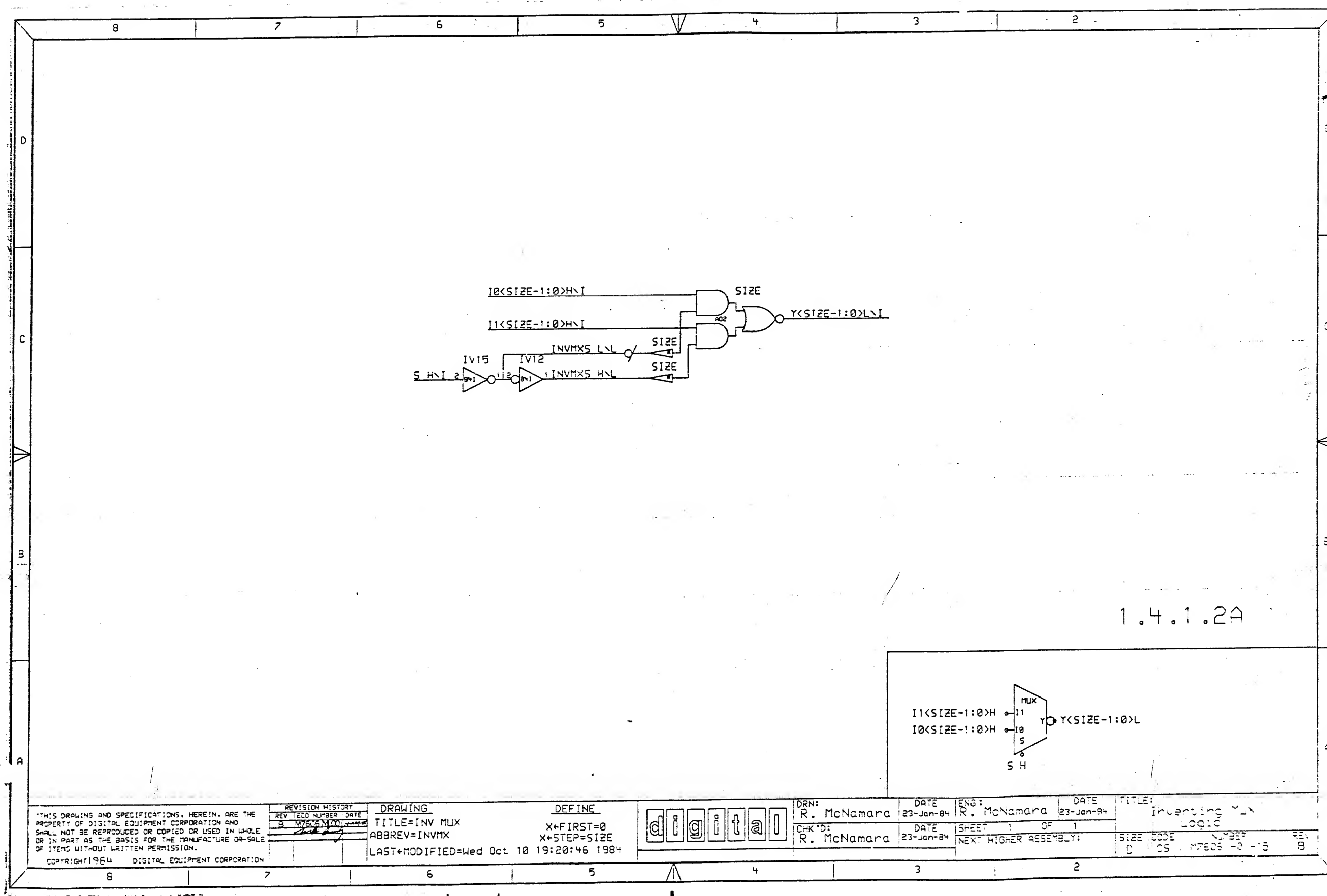
digital

DRN:
R. McNamara
CHK'D:
R. McNamara

DATE
9-NOV-83
DATE
9-NOV-83

ENG:
R. McNamara
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

TITLE:
Vector Hack
SIZE CODE
0 05 47505 -0 -4



1.4.1.2A

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REVISION HISTORY		
REV	TECD NUMBER	DATE
B	W565M001	1984

DRAWING
TITLE=INV MUX
ABBREV=INVMX
LAST*MODIFIED=Wed Oct 10 19:20:46 1984

DEFINE
X*FIRST=0
X*STEP=SIZE

digital

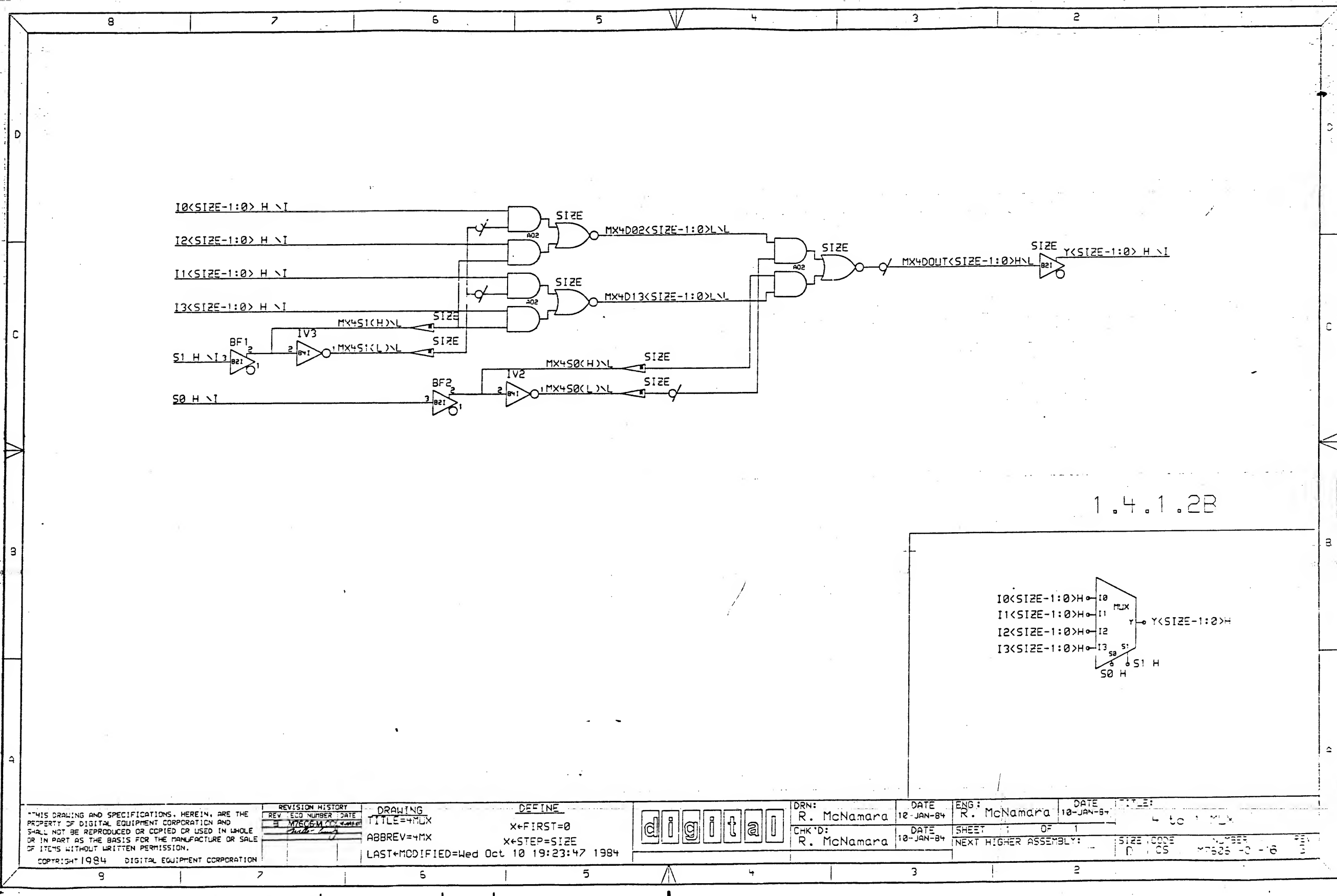
DRN:
R. McNamara
CHK'D:
R. McNamara

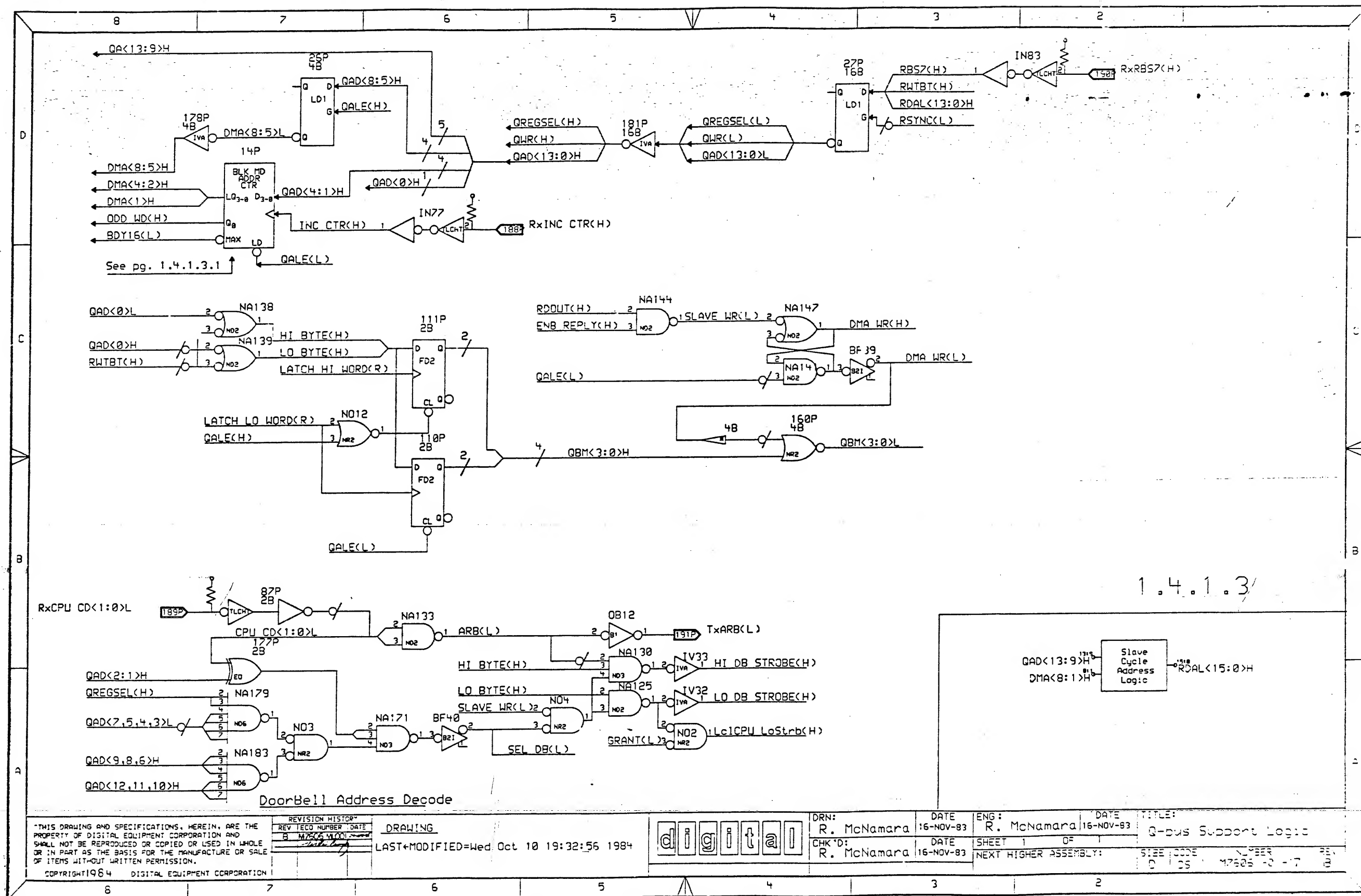
DATE
23-Jan-84
DATE
23-Jan-84

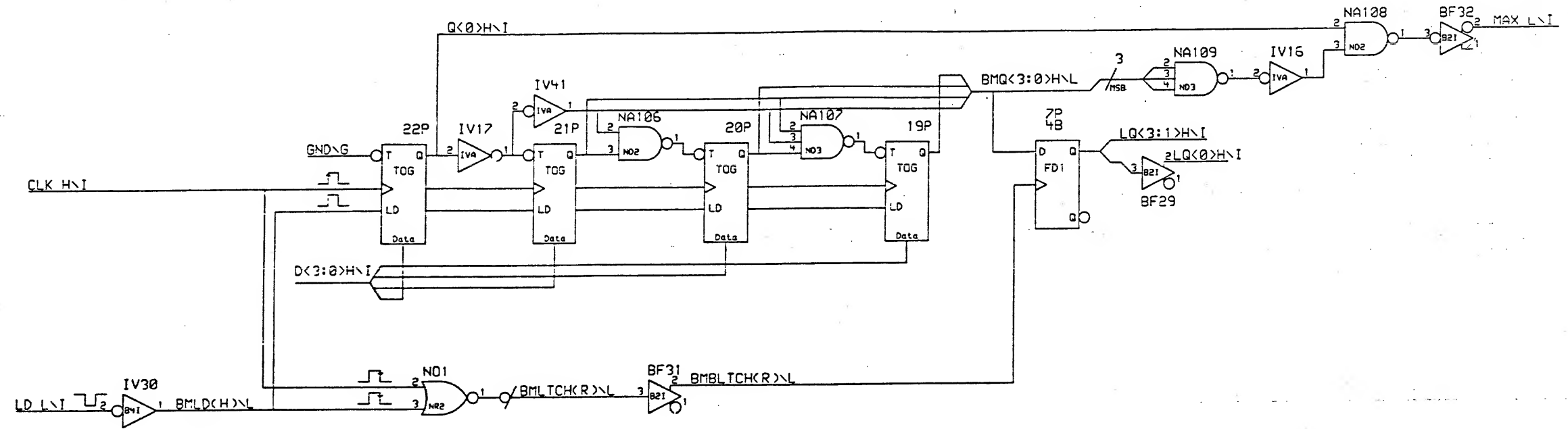
ENG:
R. McNamara
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

DATE
23-Jan-84
TITLE:
Inverting MUX Logic
SIZE CODE
D CS M7625 -2 -5

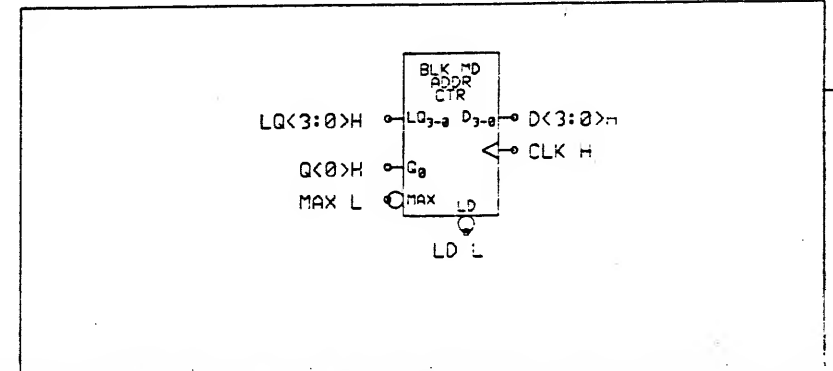
COPYRIGHT 1984 DIGITAL EQUIPMENT CORPORATION



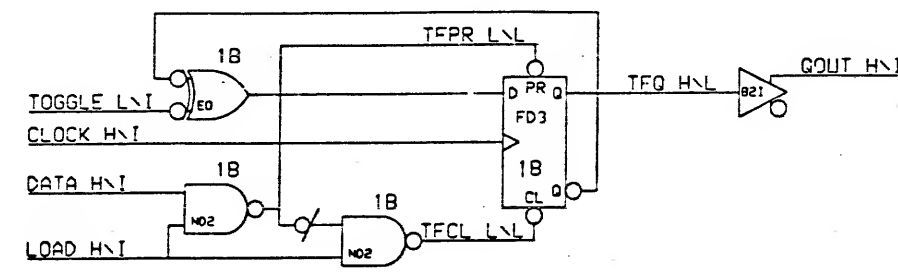




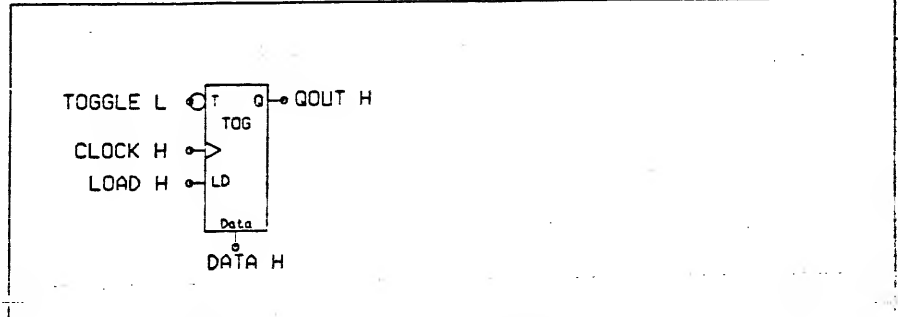
1.4.1.3.1



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									CHK'D: R. McNamara	DATE 6-NOV-83	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:	SIZE CODE D 1 CS
													NUMBER 7523-03-18
													REV. F



1.4.1.3.1.1



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REVISION HISTORY		
REV	ECO NUMBER	DATE
1	10000001	10/10/83

DRAWING
TITLE=TOG
ABBREV=TOG

DEFINE
X*FIRST=0
X*STEP=SIZE

digital

DRN: R. McNamara 6-NOV-83
CHK'D: R. McNamara 6-NOV-83

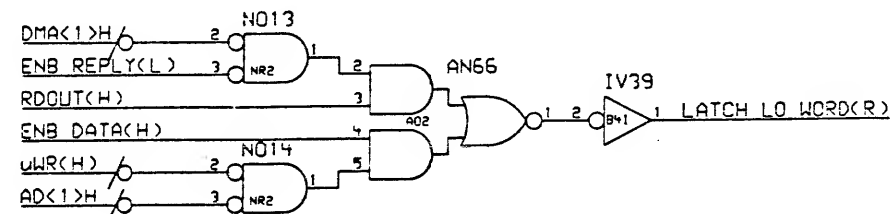
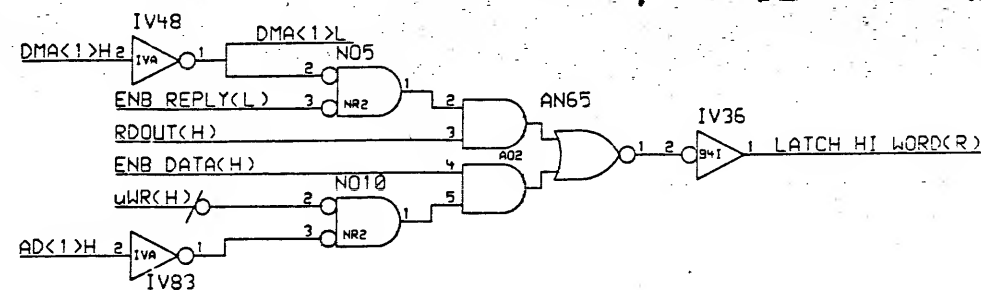
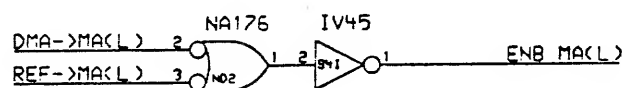
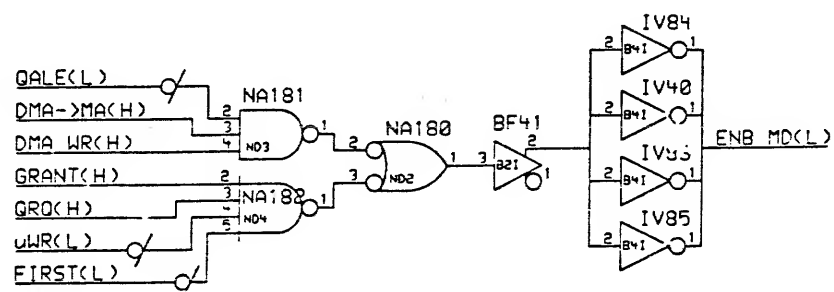
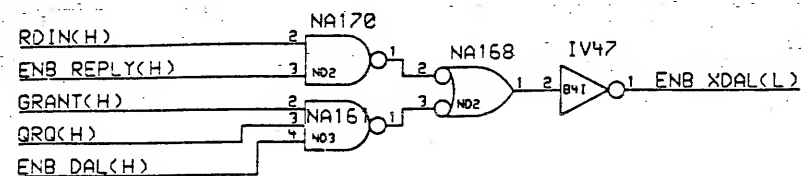
ENG: R. McNamara 6-NOV-83
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

TITLE: TOGGLE FLOP
SIZE CODE: D 05
NUMBER: 10000001

LAST MODIFIED=Wed Oct 10 19:57:28 1984

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100



1.4.1.5

Data	LATCH LO WORD(R)
Flow	LATCH HI WORD(R)
Control	LATCH MD(H)
Logic	ENB MD(L)
	ENB MAC(L)
	ENB XDAL(L)

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REV	ECO NUMBER	DATE
B	1000	10/10/84

DRAWING

LAST MODIFIED=Wed Oct 10 19:45:31 1984

digital

DRN: R. McNamara
CHK'D: R. McNamara

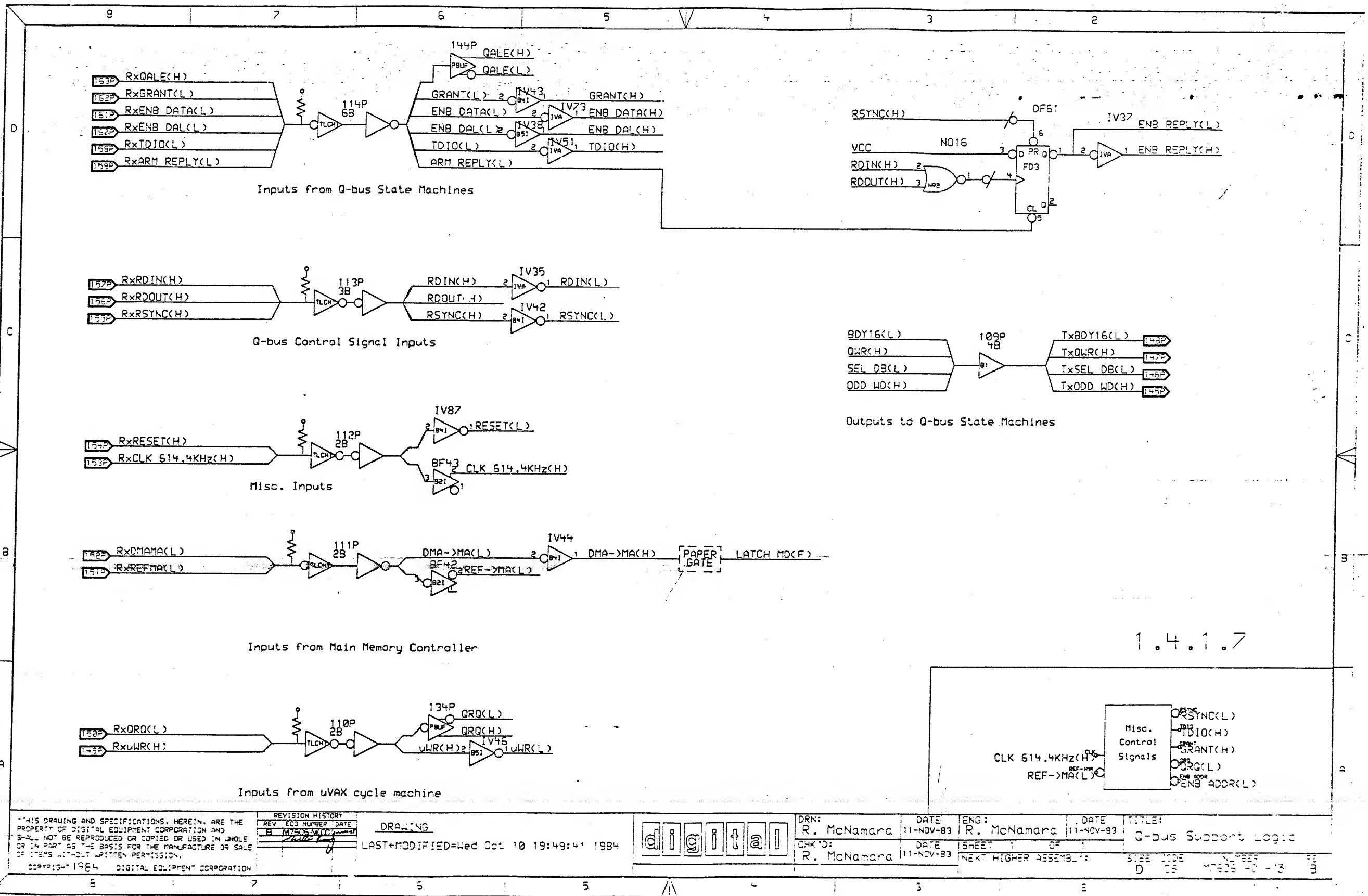
DATE 09-NOV-83
DATE 09-NOV-83

ENG: R. McNamara
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

DATE 09-NOV-83

TITLE: Q-bus Support Logic

ISSUE CODE NUMBER
D 05 17308-00-22



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REVISION HISTORY		
REV	ECO NUMBER	DATE
1	M7555 (10/10/84)	

DRAWING

LAST MODIFIED: Wed Oct 10 19:49:41 1984

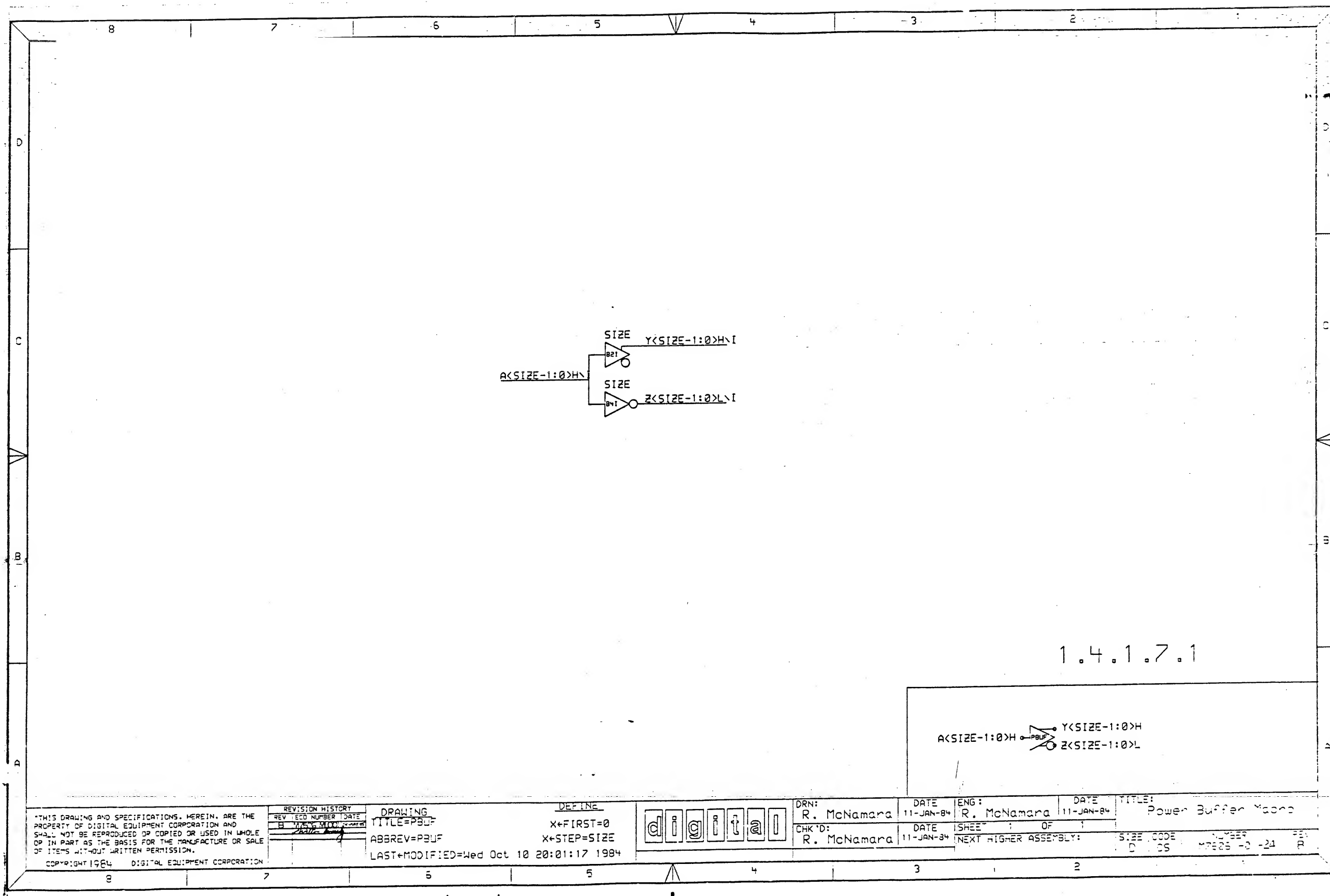
digital

DRN: R. McNamara
CHK'D: R. McNamara

DATE 11-NOV-83
DATE 11-NOV-83

ENG: R. McNamara
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

TITLE: Q-bus Support Logic
SIZE: 11x17
D 25 47628-00-13



1.4.1.7.1

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REVISION HISTORY		
REV	ECO NUMBER	DATE
1	1	11-JAN-84

DRAWING
TITLE=PSUF
ABBREV=PSUF
LAST MODIFIED=Wed Oct 10 20:01:17 1984

DEFINE
X+FIRST=0
X+STEP=SIZE

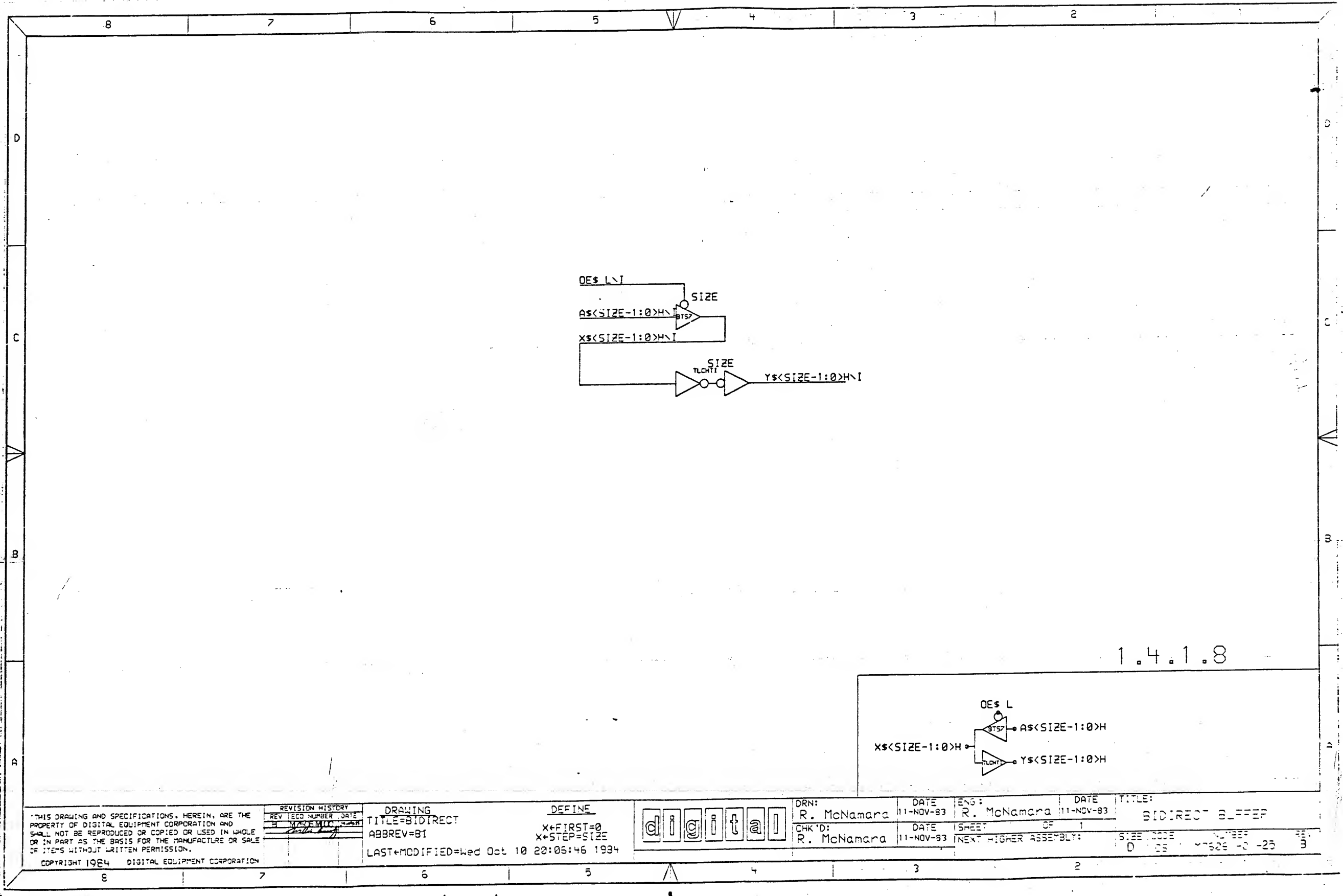
digital

DRN:
R. McNamara
CHK'D:
R. McNamara

DATE
11-JAN-84
DATE
11-JAN-84

ENG:
R. McNamara
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

TITLE:
Power Buffer Macro
SIZE CODE
D 05
NUMBER
M7225-0-24
REV
R



1.4.1.8

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REVISION HISTORY		
REV	ISSUED NUMBER	DATE
1	10-10-83	10-10-83

DRAWING
TITLE=BIDIRECT
ABBREV=81
LAST MODIFIED=Wed Oct 10 20:05:46 1984

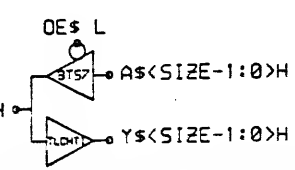
DEFINE

X+FIRST=0
X+STEP=SIZE



DRN:	R. McNamara	DATE	11-NOV-83	ENG:	R. McNamara	DATE	11-NOV-83
CHK'D:	R. McNamara	DATE	11-NOV-83	SHEET	OF		

TITLE:
BIDIRECT BLFFER

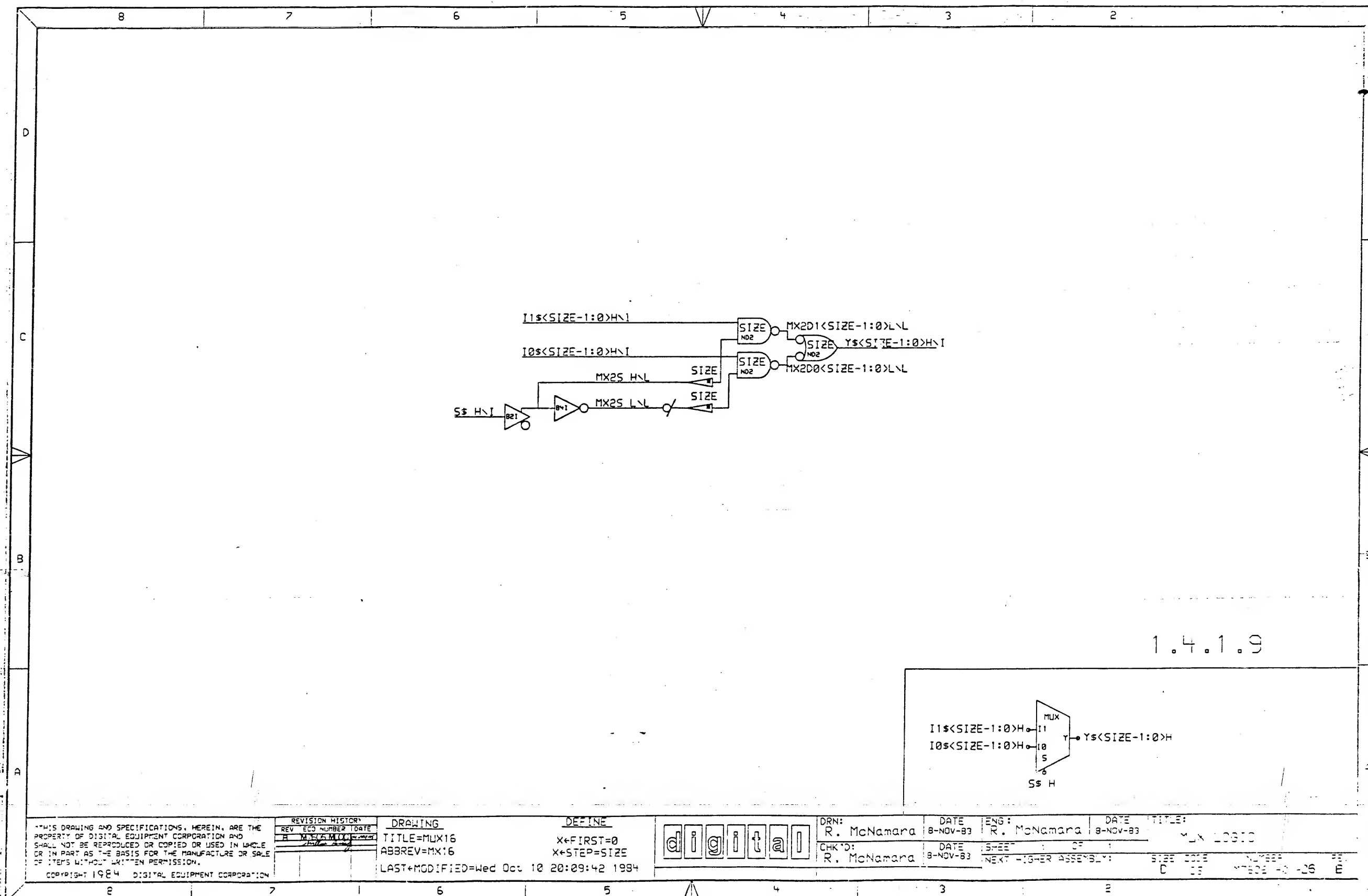


OE\$ L

A\$ < SIZE-1:0> H

X\$ < SIZE-1:0> H

Y\$ < SIZE-1:0> H



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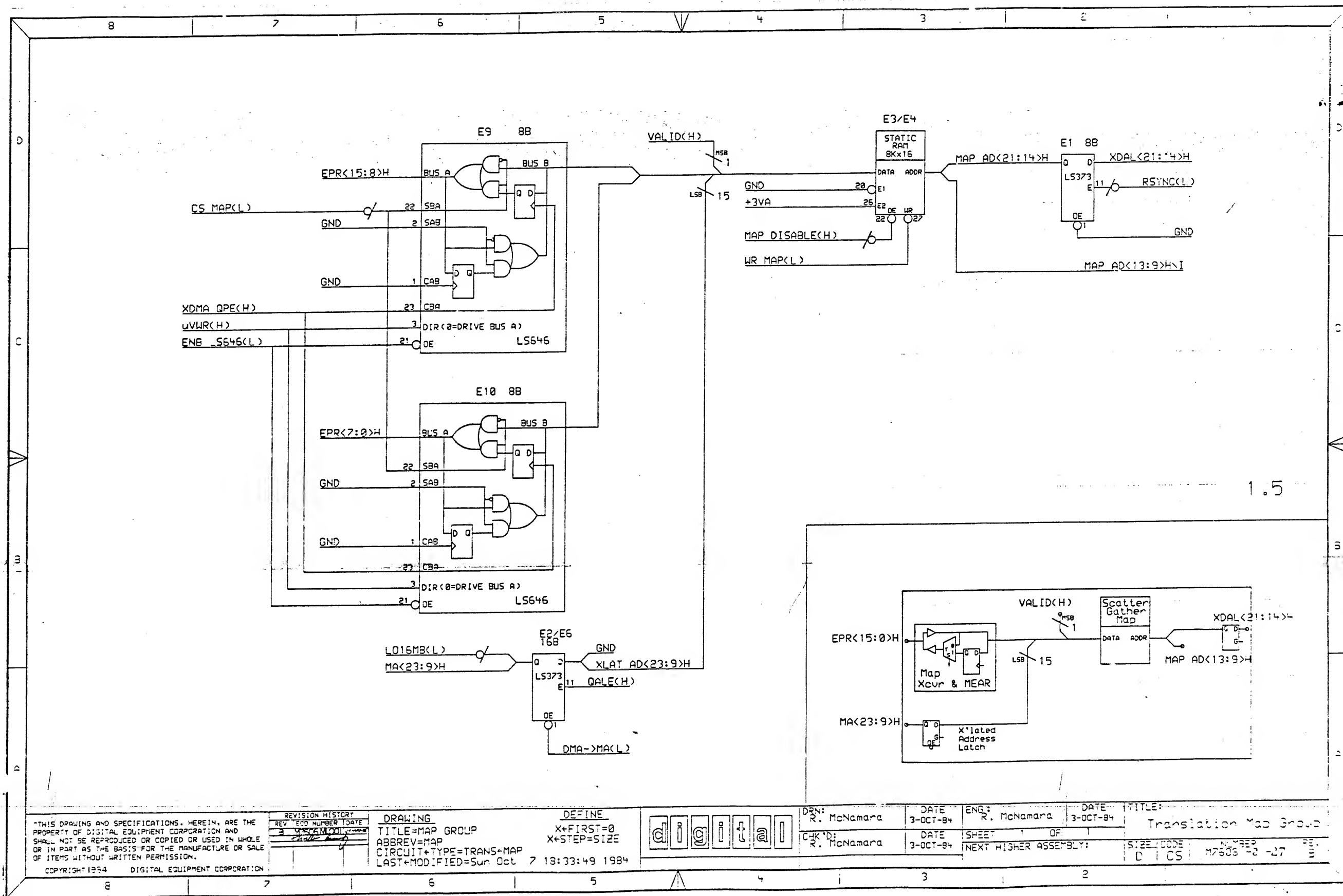
REVISION HISTORY		
REV	ECO NUMBER	DATE
1	1	11/08/83

DRAWING
TITLE=MUX16
ABBREV=MX16
LAST*MODIFIED=Wed Oct 10 20:09:42 1994

DEFINE
X*FIRST=0
X*STEP=SIZE

digital

DRN:	R. McNamara	DATE	8-NOV-83	ENG:	R. McNamara	DATE	8-NOV-83	TITLE:	MUX LOGIC
CHK'D:	R. McNamara	DATE	8-NOV-83	SHEET	1	OF	1	SIZE CODE	C
NEXT HIGHER ASSEMBLY:				NUMBER		125			



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REV	ECO NUMBER	DATE
1	1	10/7/84

DRAWING
 TITLE=MAP GROUP
 ABBREV=MAP
 CIRCUIT+TYPE=TRANS+MAP
 LAST+MODIFIED=Sun Oct 7 18:33:49 1984

DEFINE
 X+FIRST=0
 X+STEP=SIZE

digital

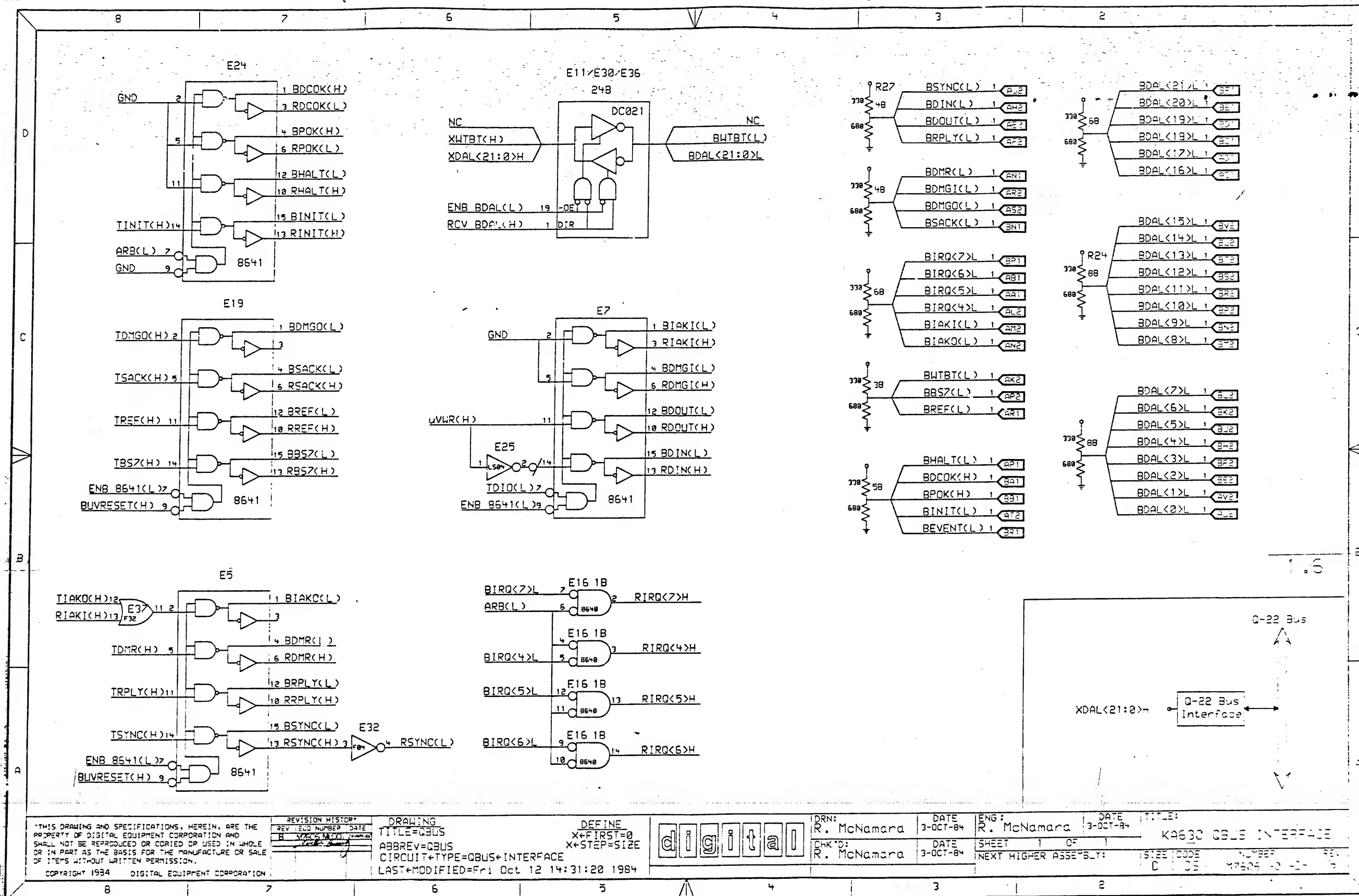
DRN: R. McNamara
 CHK'D: R. McNamara

DATE 3-OCT-84
 DATE 3-OCT-84

ENG: R. McNamara
 SHEET 1 OF 1

DATE 3-OCT-84
 NEXT HIGHER ASSEMBLY:

TITLE:
 Translation Map Group
 SIZE/ CODE D CS M7605 -2 -27



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REVISION HISTORY	DATE
REVISED NUMBER	DATE
1	10/12/84

DRAWING
TITLE=QBUS
ABBREV=QBUS
CIRCUIT+TYPE=QBUS+INTERFACE
LAST+MODIFIED=Fri Oct 12 14:31:20 1984

DEFINE
X+FIRST=0
X+STEP=SIZE

digital

DRN:
R. McNamara
DATE
3-OCT-84

CHK'D:
R. McNamara
DATE
3-OCT-84

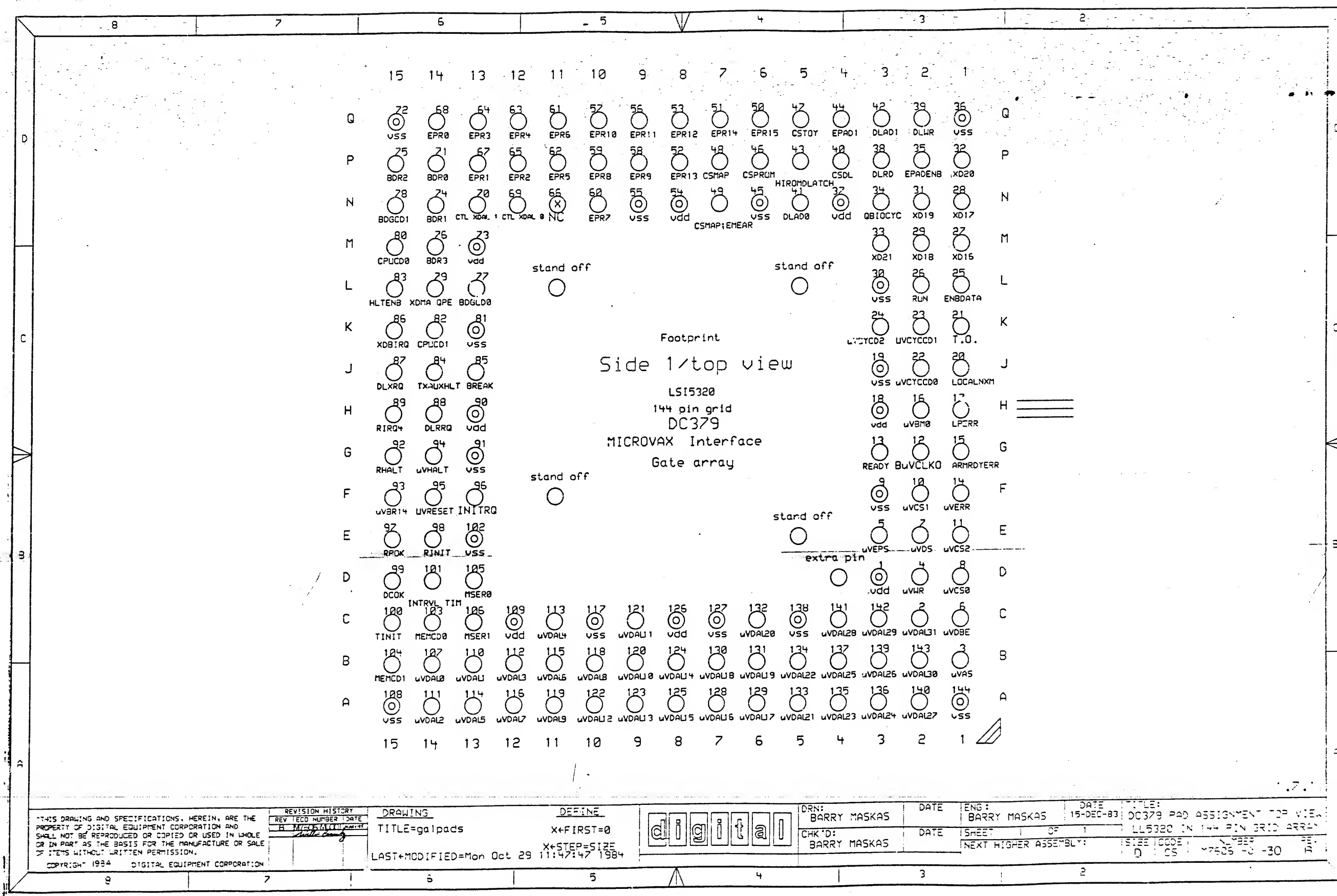
ENG:
R. McNamara
DATE
3-OCT-84

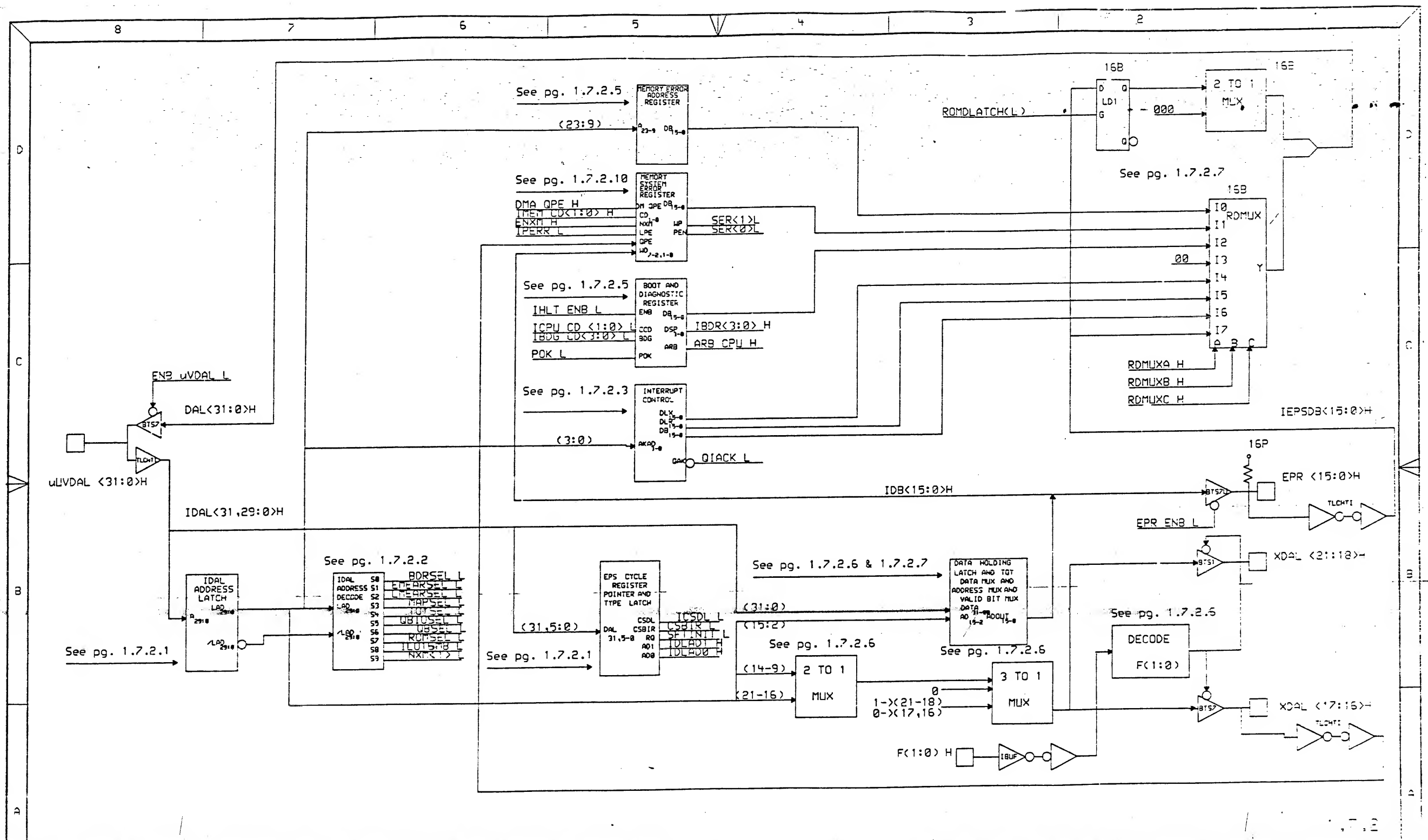
SHEET 1 OF 1

NEXT HIGHER ASSEMBLY:

TITLE:
K4630 QBUS INTERFACE

SIZE CODE
C 05 17505 40 1-1





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REVISION HISTORY		
REV	ECO NUMBER	DATE
1	1	10/7/84

DRAWING
 TITLE=GA1BLOCK
 ABBREV=GA1BLOCK
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Sun Oct 7 20:17:53 1984

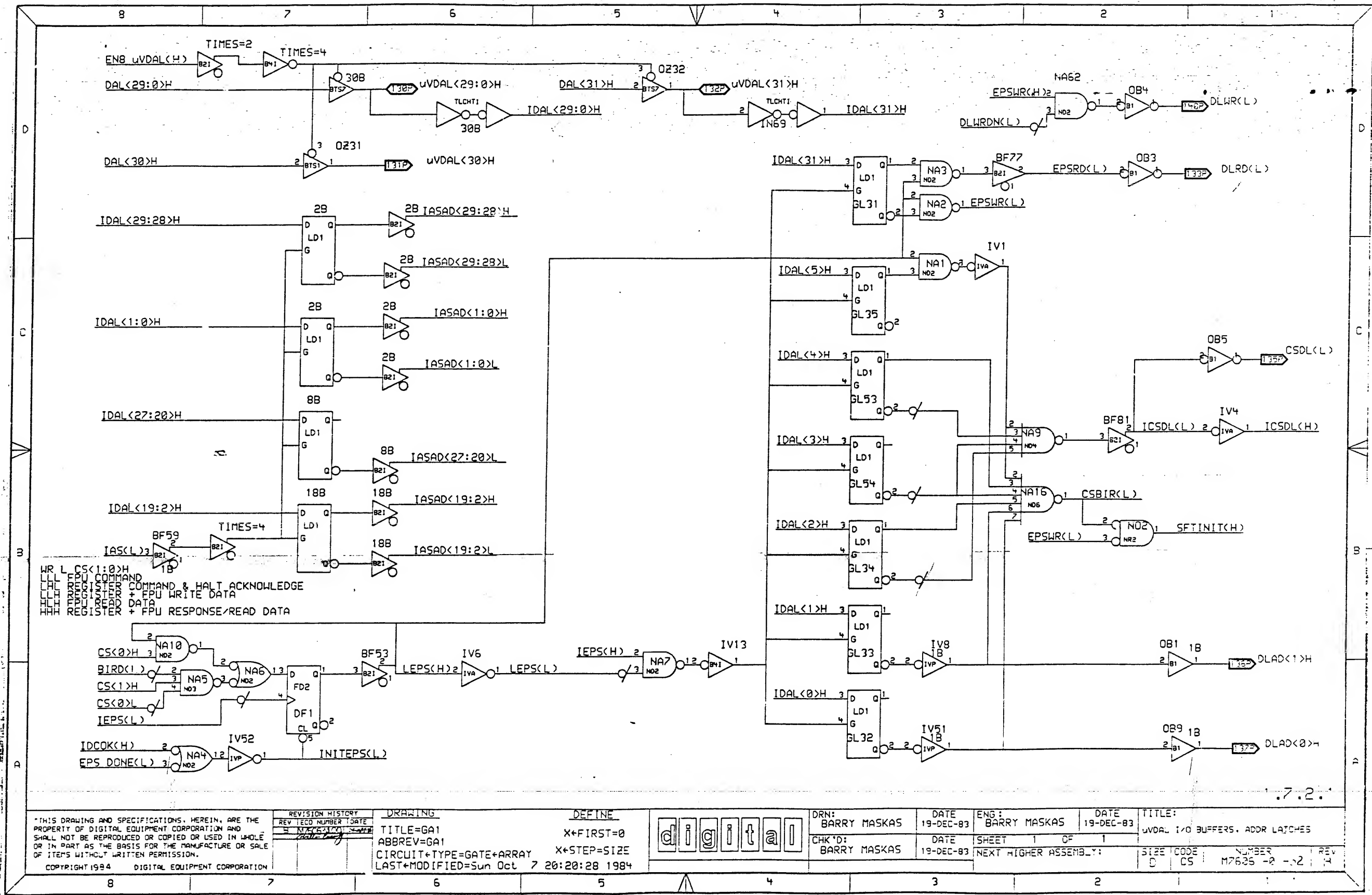
digital

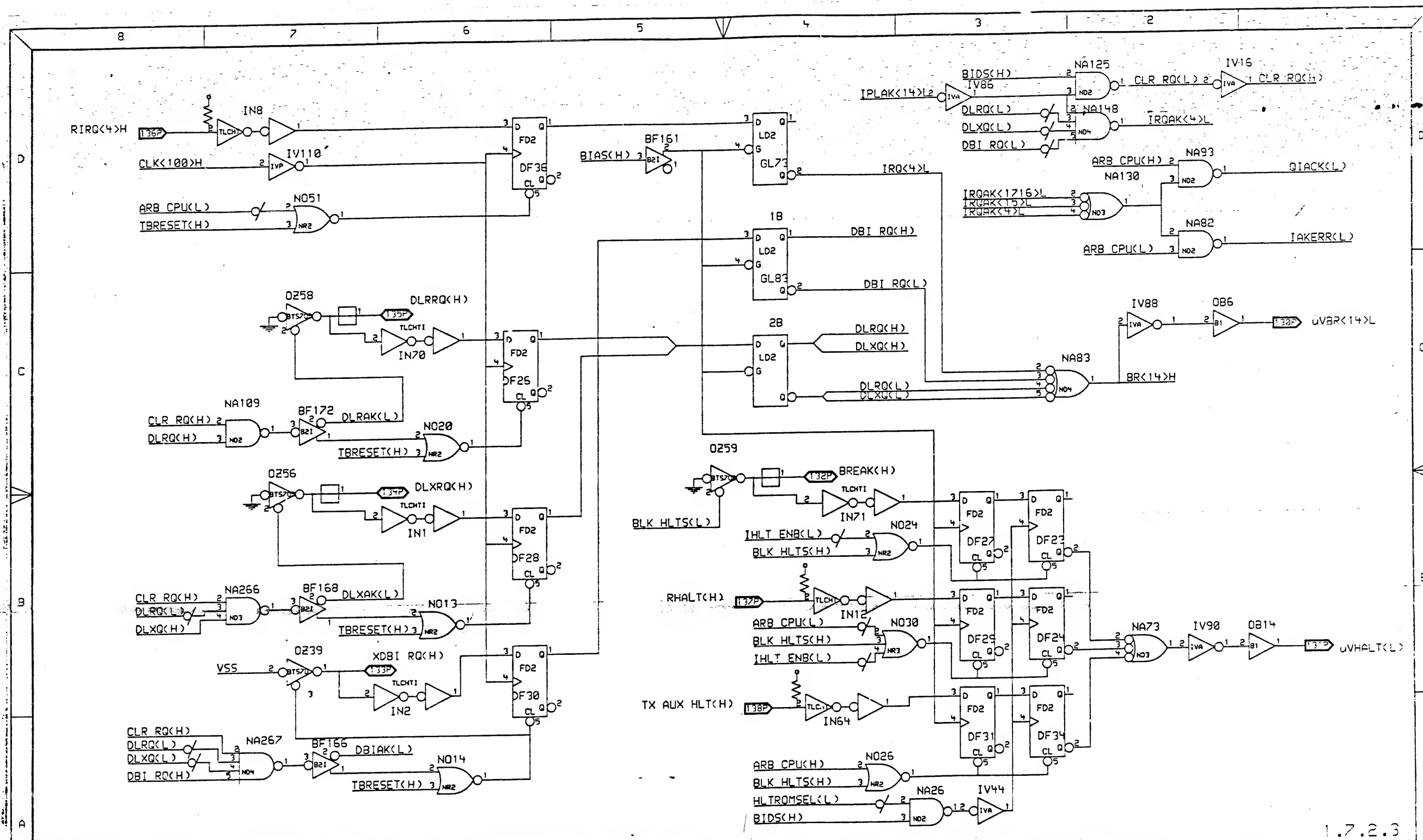
DRN: BARRY MASKAS
 CHK'D: BARRY MASKAS

DATE 15-DEC-83
 DATE 15-DEC-83

ENG: BARRY MASKAS
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

DATE 15-DEC-83
 TITLE: uvax Interface Gate Array
 Data Path
 SIZE: 10000
 M7525-10-1





1.7.2.3

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REVISION HISTORY		
REV	ECO	NUMBER DATE
1	1	11/18/83

DRAWING

TITLE=GA1

ABBREV=GA1

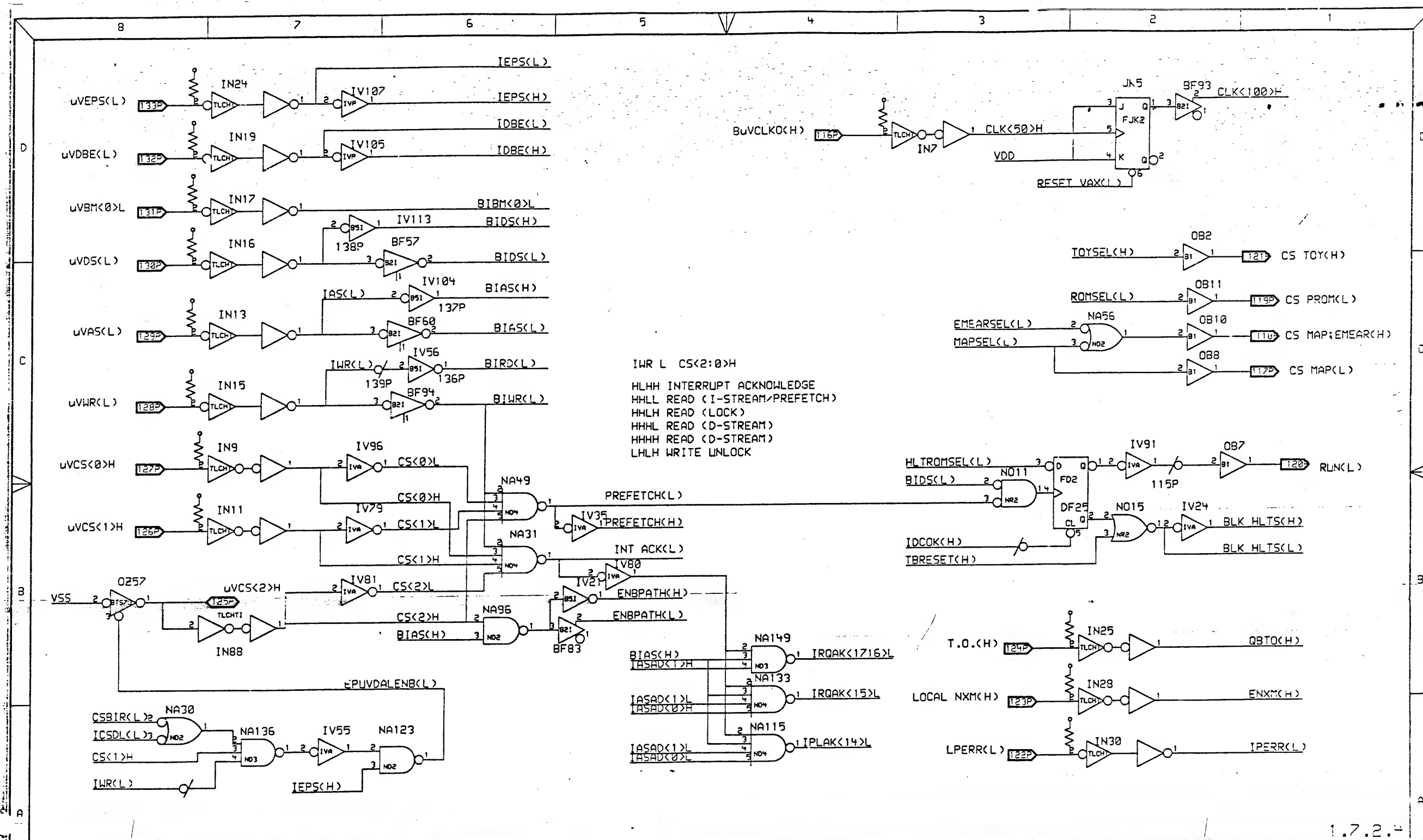
CIRCUIT+TYPE=GATE+ARRAY

LAST+MODIFIED=Sun Oct 7 16:40:03 1984

digital

DRN:	BARRY MASKAS	DATE	18-DEC-83
CHK'D:	BARRY MASKAS	DATE	18-DEC-83
SHEET		1	OF 1
NEXT HIGHER ASSEMBLY:			

TITLE:		EXCEPTIONS AND INTERRUPTS
SIZE	CODE	NUMBER
D	CS	M7506-2-3



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REVISION HISTORY		
REV	ECG NUMBER	DATE
1	1000	10-20-83

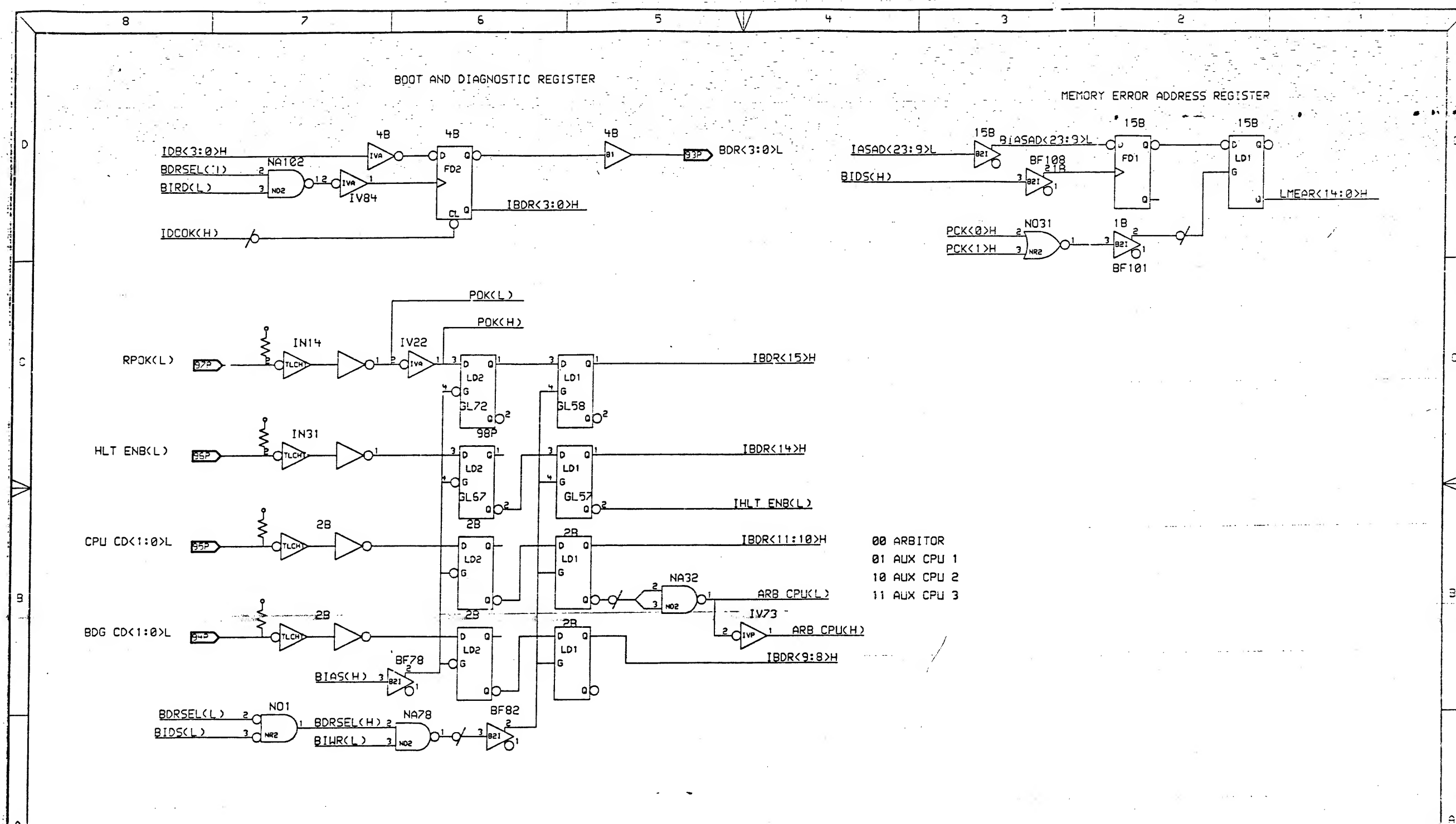
DRAWING
TITLE=GA1
ABBREV=GA1
CIRCUIT+TYPE=GATE+ARRAY
LAST+MODIFIED=Sat Oct 20 18:44:09 1984

digital

DRN: BARRY MASKAS
CHK'D: BARRY MASKAS
DATE 19-DEC-83
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

ENG: BARRY MASKAS
DATE 19-DEC-83
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

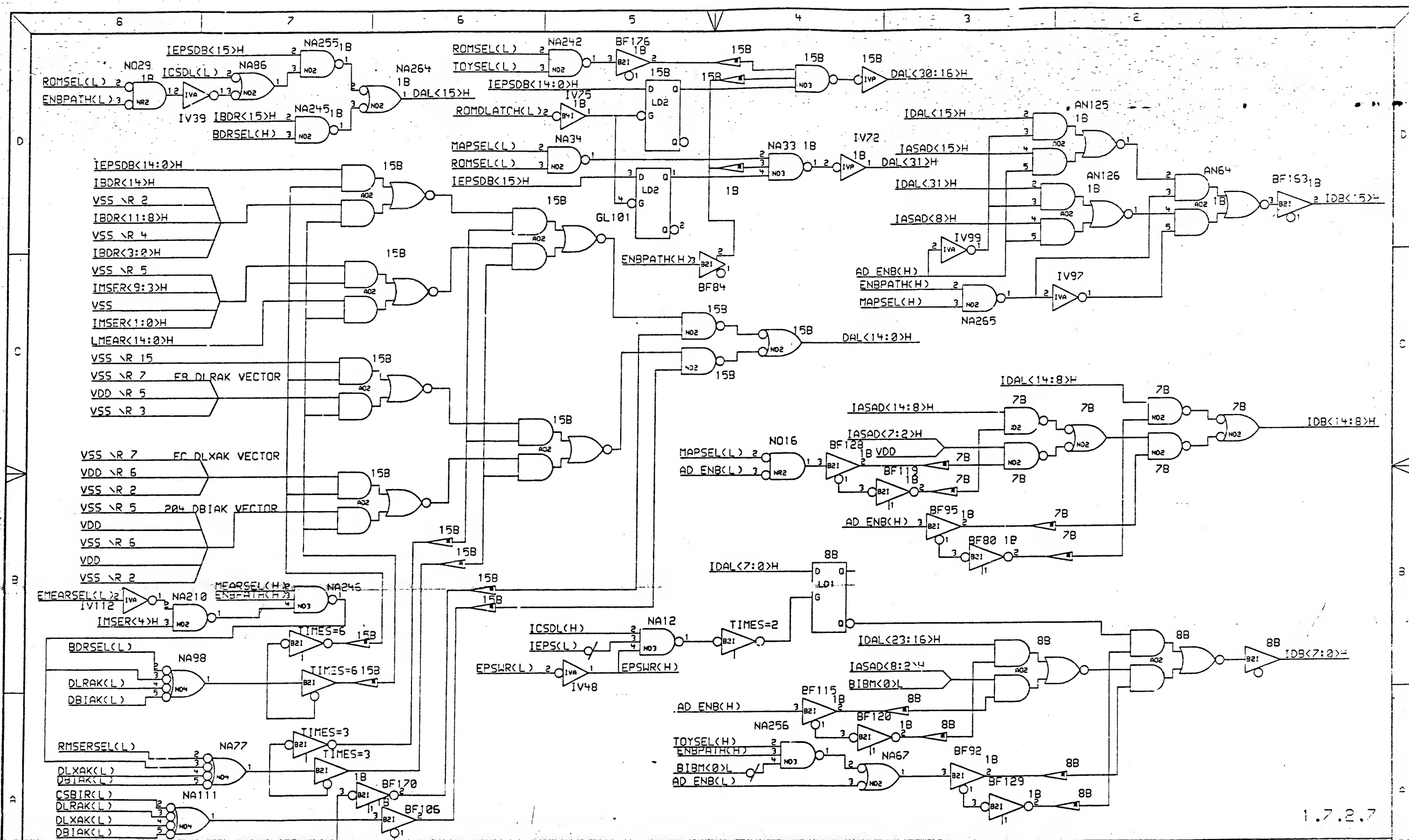
TITLE: UVAX INPUTS AND I/O PINS
SIZE D CODE CS NUMBER M7635 -0 -35 REV 3



- 00 ARBITOR
- 01 AUX CPU 1
- 10 AUX CPU 2
- 11 AUX CPU 3

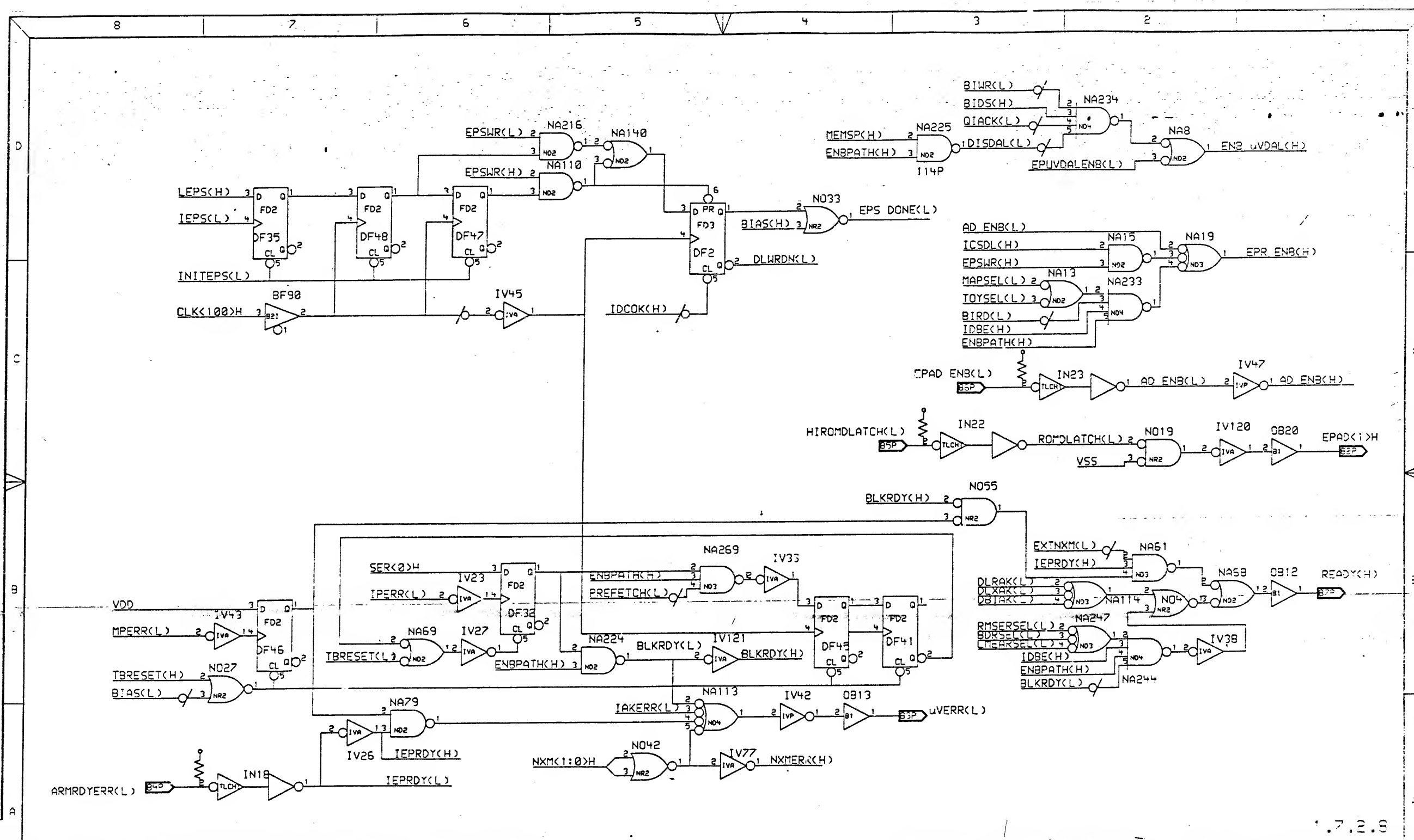
1.7.2.5

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	digital		CHK'D: BARRY MASKAS DATE 18-DEC-83		SHEET 1 OF 1		NEXT HIGHER ASSEMBLY:		SIZE: CCDE 0 C5	
	NUMBER M7606 -0 -35		REV 1		1		1		1	
	1		1		1		1		1	



1.7.2.7

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COPYRIGHT 1984 DIGITAL EQUIPMENT CORPORATION		REV. TECH. NUMBER DATE		TITLE=GA1				CHK'D: BARRY MASKAS	DATE: 19-DEC-83	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:	SIZE CODE NUMBER
				CIRCUIT+TYPE=GATE+ARRAY								D C5 17525 -0 -38 3
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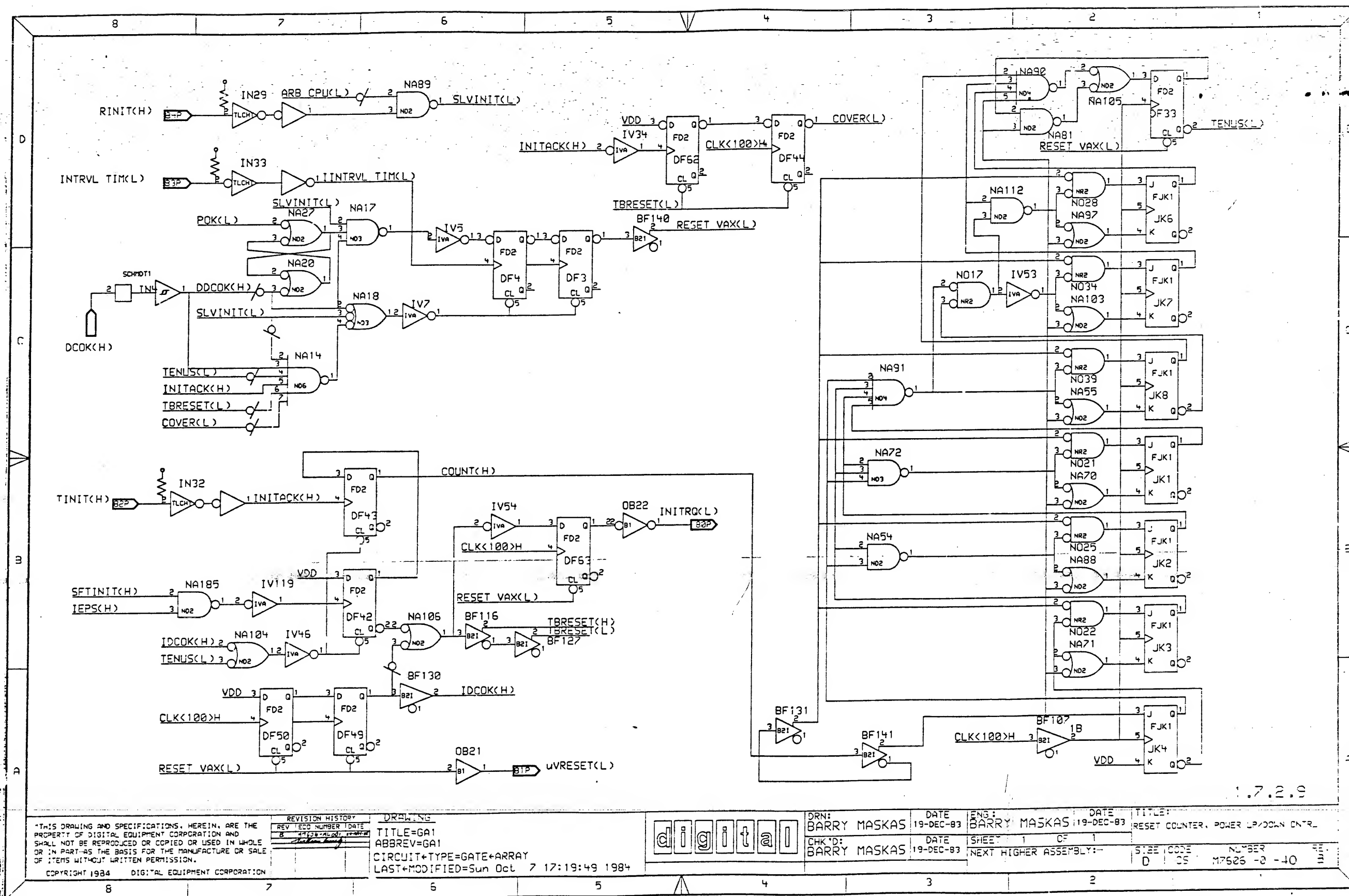
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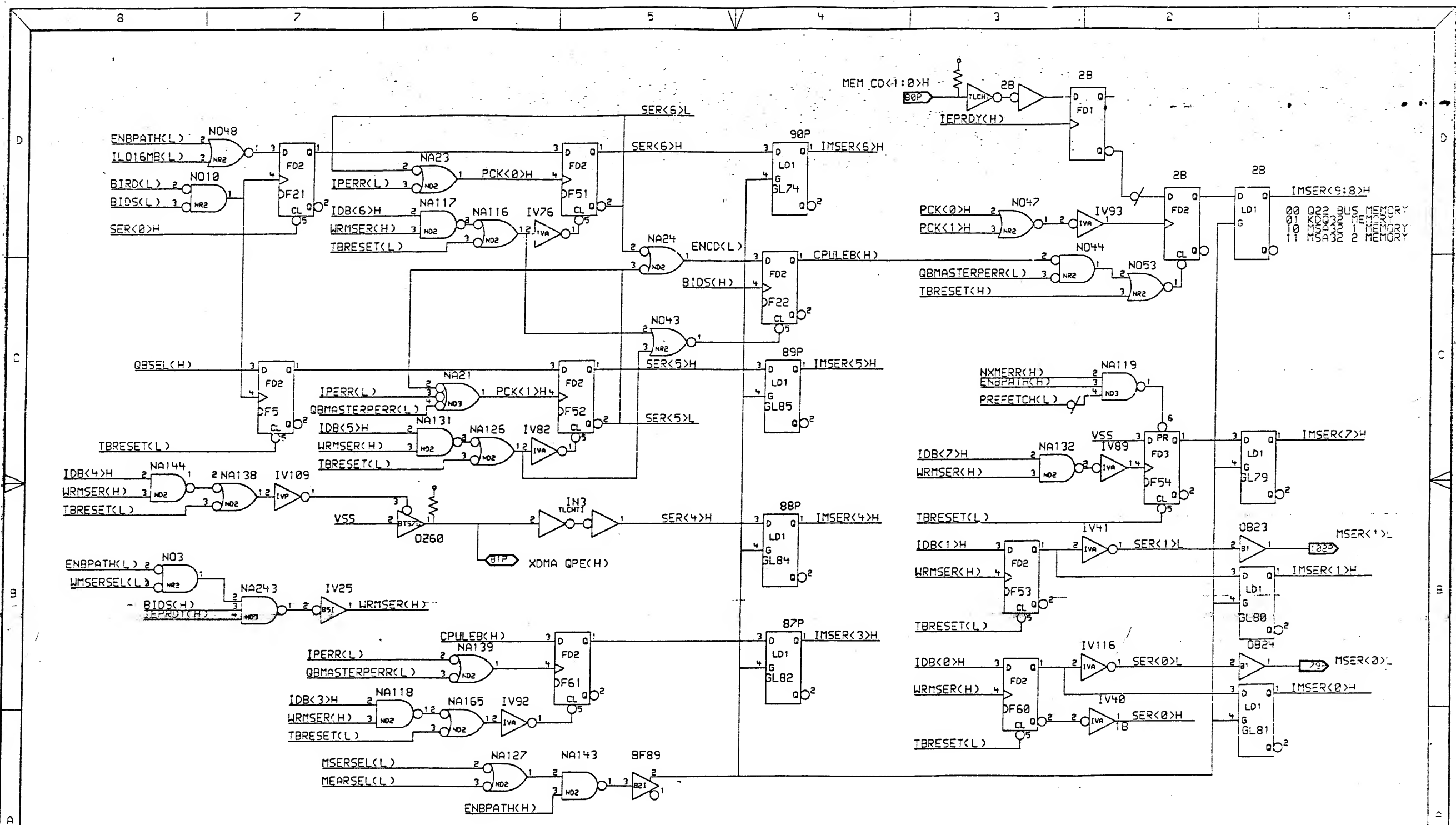
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REVISION HISTORY			DRAWING	
REV	ECN	NUMBER	DATE	
1			11/18/83	GA
2			12/15/83	GA

TITLE=GA:
 ABBREV=GA:
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Sun Oct 7 17:15:18 1984

digit		DRN: BARRY MASKAS	DATE: 19-DEC-83	ENG: BARRY MASKAS	DATE: 19-DEC-83	TITLE: MISC. CONTROL STROBES
		CHK'D: BARRY MASKAS	DATE: 19-DEC-83	SHEET 1 OF 1		
		NEXT HIGHER ASSEMBLY:		SIZE CODE: D CS		NUMBER: 47626 -2 -09





1.7.2.12

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REV	ECO NUMBER	DATE
0	1760-ALG01	11/1/84

DRAWING
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ABBREV=GA1
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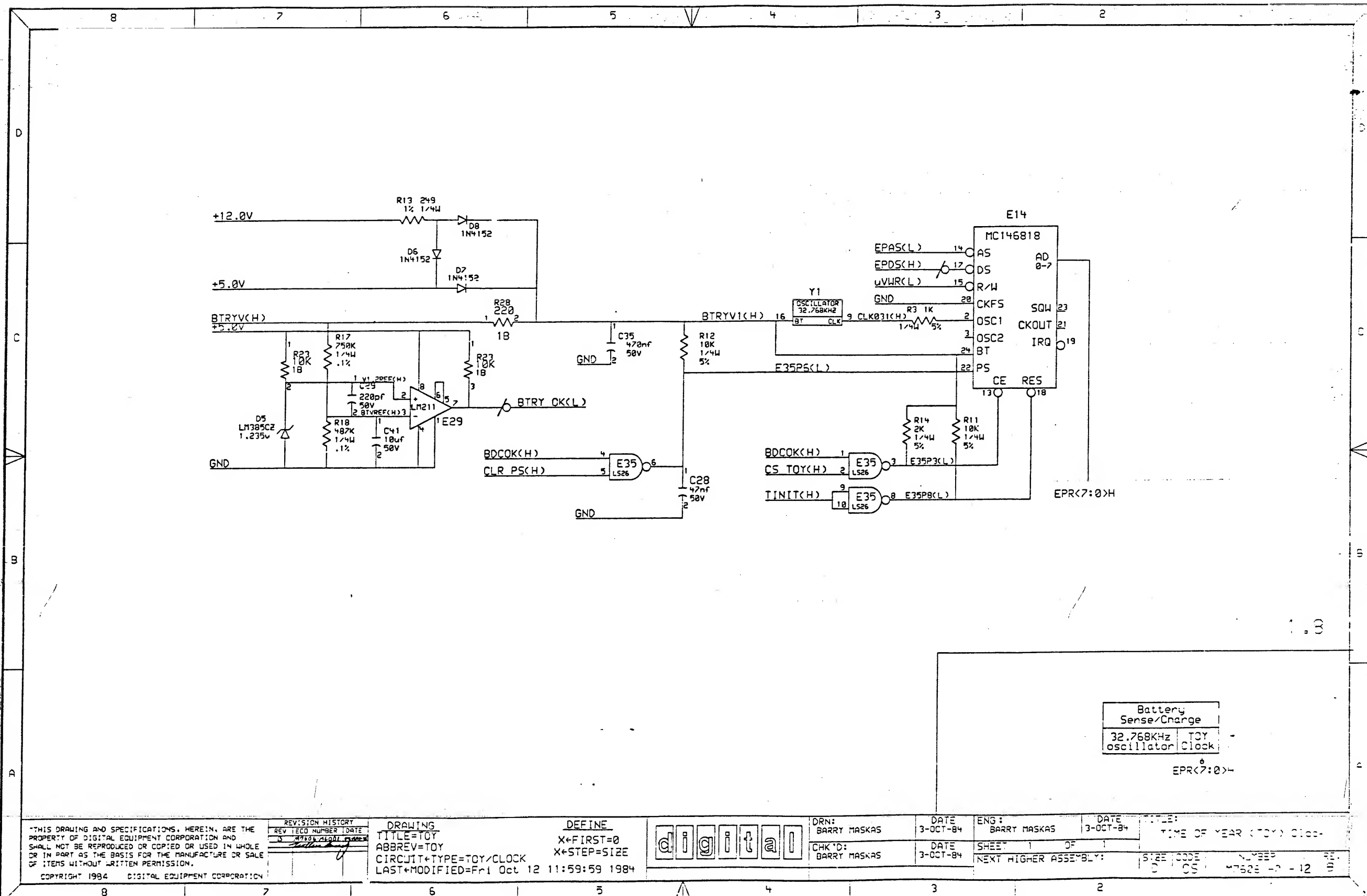
digital

DRN: BARRY MASKAS
CHK'D: BARRY MASKAS

DATE 19-DEC-83
DATE 19-DEC-83

ENG: BARRY MASKAS
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

TITLE: MEMORY SYSTEM ERROR REGISTER
SIZE CODE D 1 CS
NUMBER M7505 -2 -41
REV. F



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REVISION HISTORY		
REV	ECO NUMBER	DATE
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DRAWING
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ABBREV=TOY
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LAST+MODIFIED=Fr1 Oct 12 11:59:59 1984

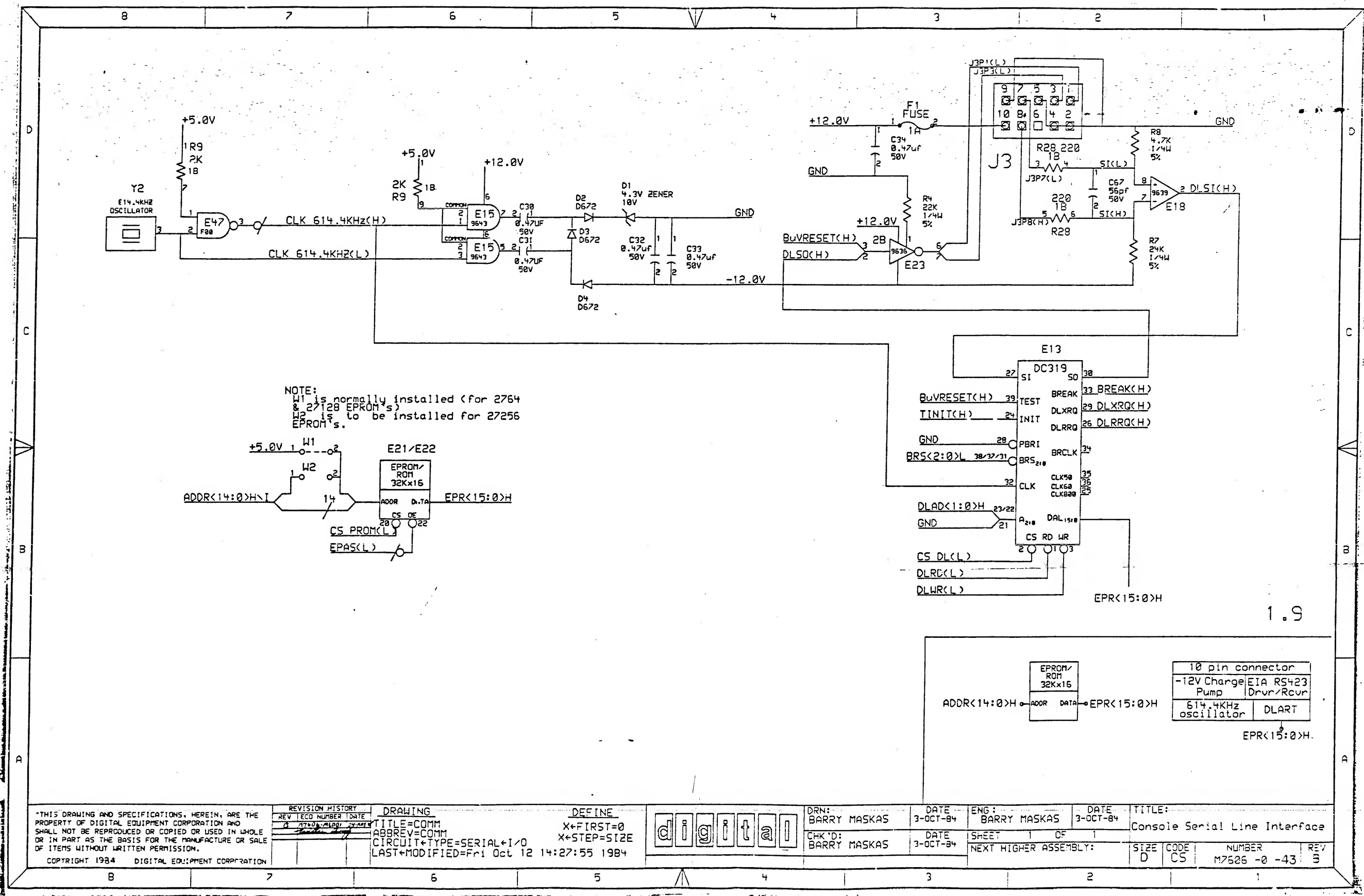
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X+STEP=SIZE

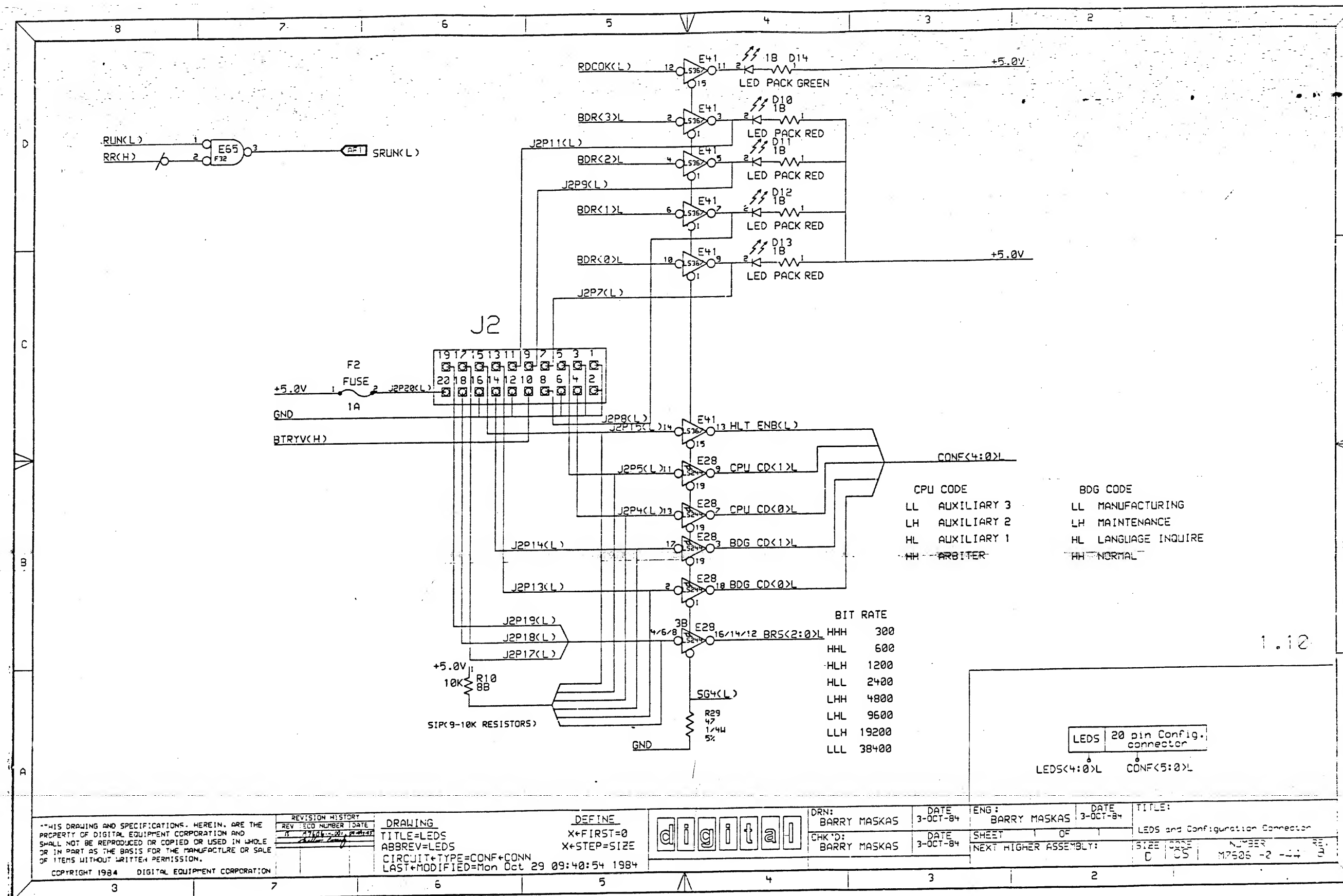


DRN: BARRY MASKAS	DATE 3-OCT-84
CHK'D: BARRY MASKAS	DATE 3-OCT-84

ENG: BARRY MASKAS	DATE 3-OCT-84
SHEET 1 OF 1	
NEXT HIGHER ASSEMBLY:	

TITLE: TIME OF YEAR (TOY) CLOCK	
SIZE CODE	NUMBER
0 CS	7525 - 12





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REVISION HISTORY		
REV	ECO NUMBER	DATE
1	1	10/29/84

DRAWING
 TITLE=LEDS
 ABBREV=LEDS
 CIRCUIT+TYPE=CONF+CONN
 LAST+MODIFIED=Mon Oct 29 09:40:54 1984

DEFINE
 X+FIRST=0
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digital

DRN: BARRY MASKAS
 CHK'D: BARRY MASKAS

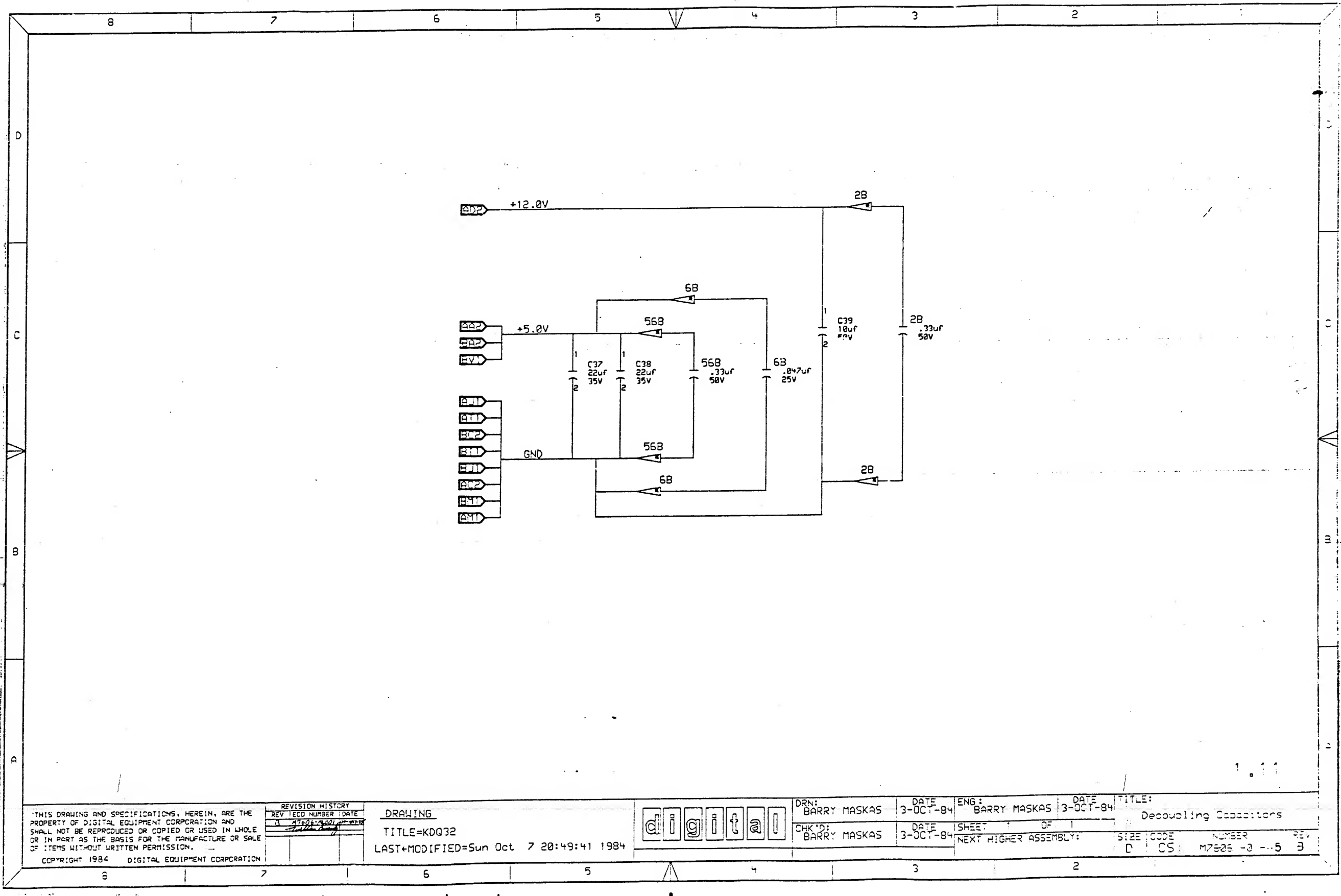
DATE: 3-OCT-84
 DATE: 3-OCT-84

ENG: BARRY MASKAS
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

DATE: 3-OCT-84

TITLE:
 LEDS and Configuration Connector

SIZE: 0 05 NUMBER: M7505 -2 -44



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REVISION HISTORY		
REV	ECO NUMBER	DATE
01	17808-1-001	05-01-84

DRAWING
TITLE=KDQ32
LAST*MODIFIED=Sun Oct 7 20:49:41 1984



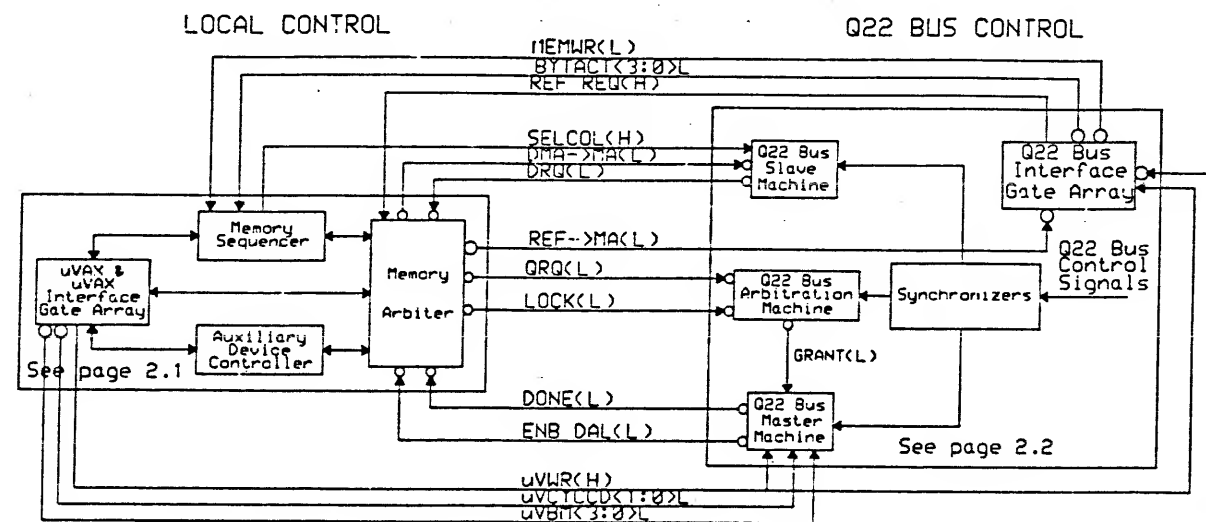
DRN: BARRY MASKAS
CHK'D: BARRY MASKAS

DATE 3-OCT-84
DATE 3-OCT-84

ENG: BARRY MASKAS
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

DATE 3-OCT-84

TITLE: Decoupling Capacitors
SIZE CODE NUMBER REV
D CS M7525 -3 -5 3



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REVISION HISTORY
REV 1 ECO NUMBER DATE
0 10-29-84 10-29-84

DRAWING

TITLE=CTLBLOCK
ABBREV=ct1
CIRCUIT+TYPE=CONTROL
LAST*MODIFIED=Mon Oct 29 09:44:18 1984

digital

DRN: BARRY MASKAS

DATE 8-DEC-83

ENG: BARRY MASKAS

DATE 8-DEC-83

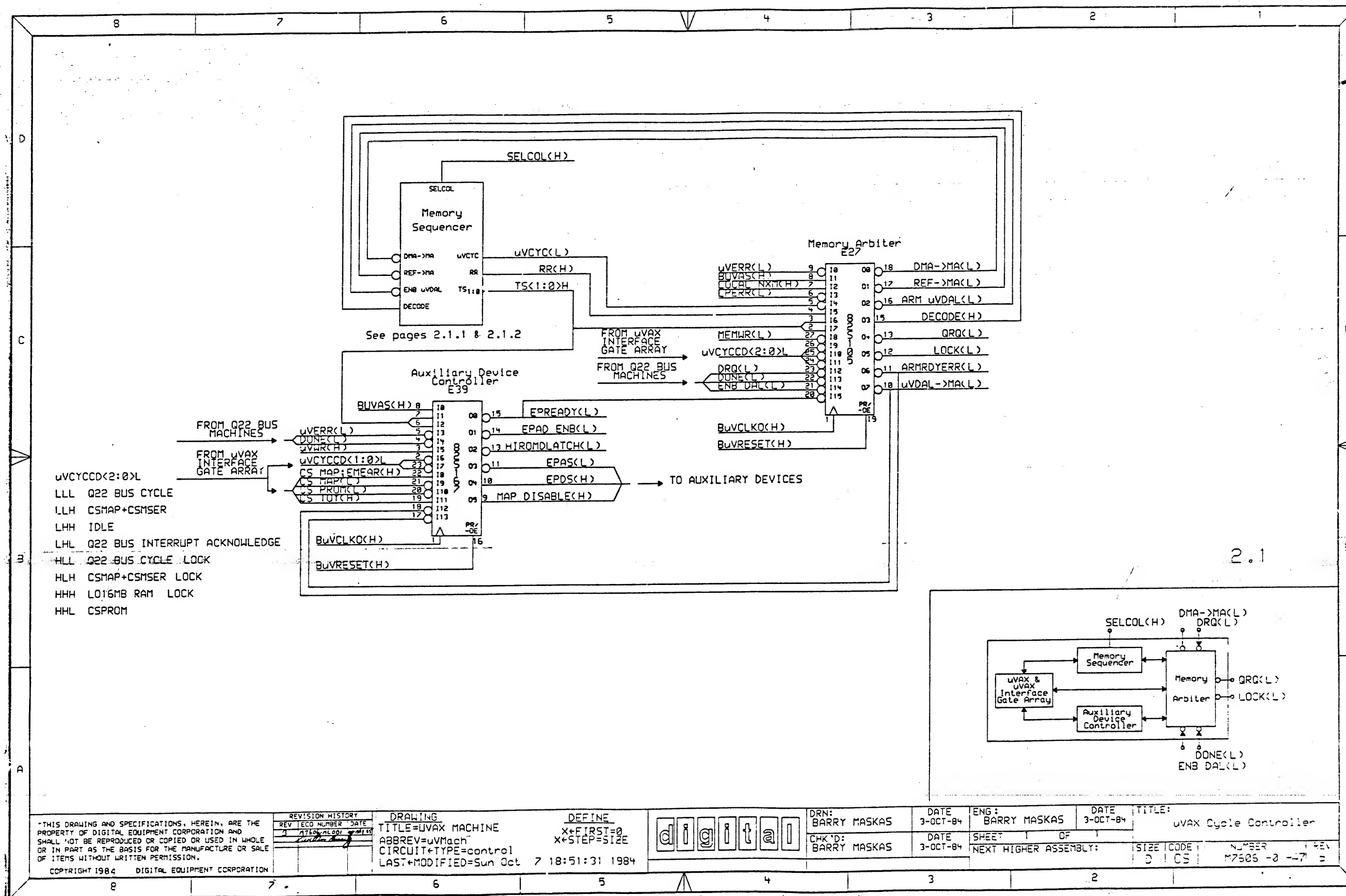
TITLE: KA630 State Machines

CHK'D: R. MCNAMARA

DATE 9-DEC-83

SHEET 07
NEXT HIGHER ASSEMBLY:

SIZE CODE NUMBER REV
1 CS M7505 -0 -46 3



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REV	ECO NUMBER	DATE
1	1760	10/1/84

DRAWING
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 ABBREV=uVMach
 CIRCUIT+TYPE=control
 LAST+MODIFIED=Sun Oct 7 18:51:31 1984

DEFINE
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 X+STEP=SIZE

digital

DRN:
BARRY MASKAS
 CHK'D:
BARRY MASKAS

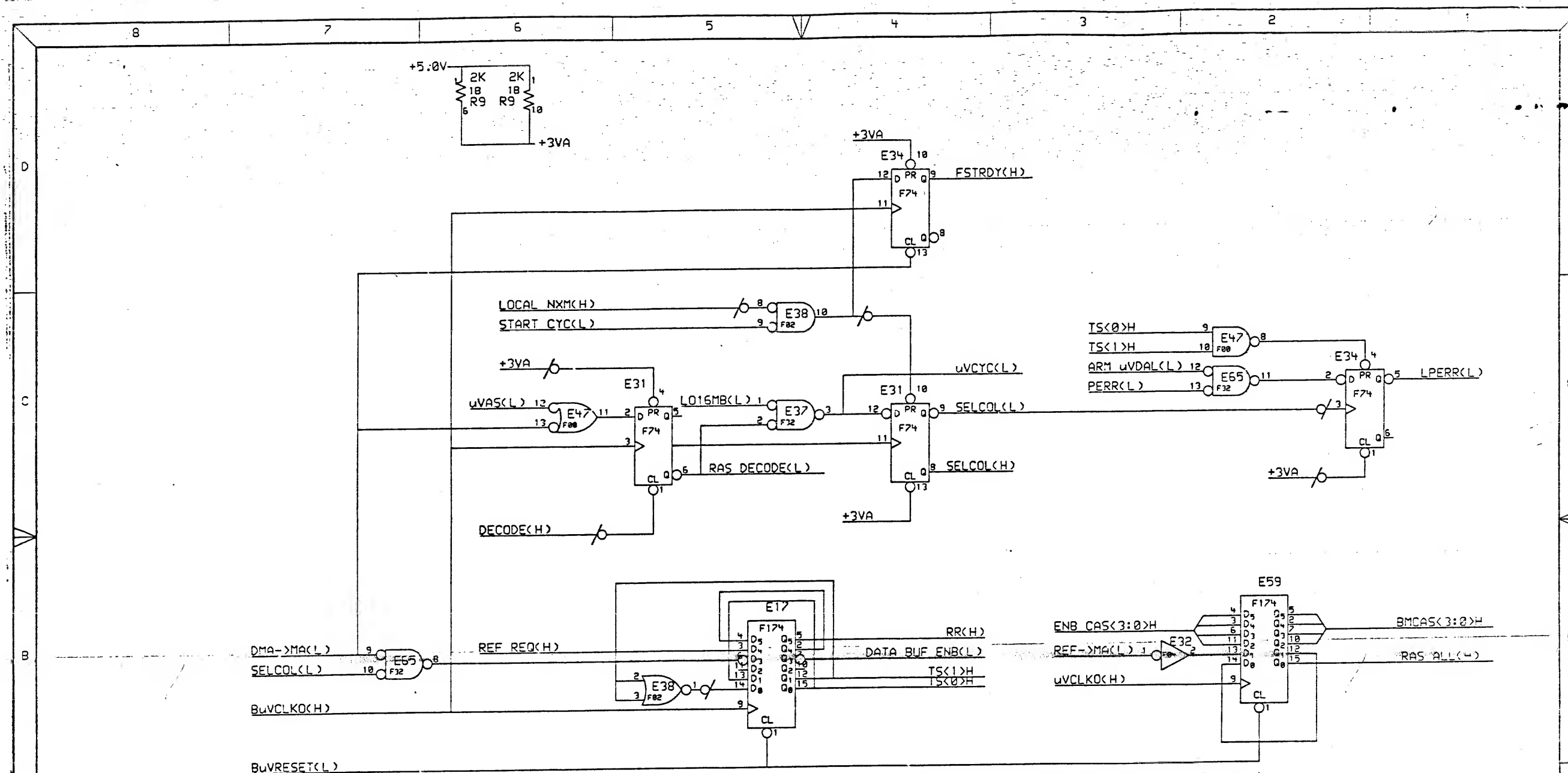
DATE
3-OCT-84
 DATE
3-OCT-84

ENG:
BARRY MASKAS
 SHEET
NEXT HIGHER ASSEMBLY:

DATE
3-OCT-84
 OF

TITLE:
 uvax Cycle Controller

SIZE CODE NUMBER REV
 D CS M7585 -0 -47 =



TS<1:0> STATE TABLE (uVAX Microcycle Counter)

s	ns	
T4	00 01	first uVAX CLK0 after BuVRESET
T1	01 11	
T2	11 10	
T3	10 00	

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REV	ECO	NUMBER	DATE
1			

DRAWING

TITLE=MEM CTRLR

ABBREV=MEMCTRL

CIRCUIT+TYPE=MEM+CTRL

LAST+MODIFIED=Fri Oct 12 14:23:21 1984

digital

DRN: BARRY MASKAS

CHK'D: BARRY MASKAS

DATE 18-DEC-83

DATE 18-DEC-83

ENG: BARRY MASKAS

SHEET 1 OF 1

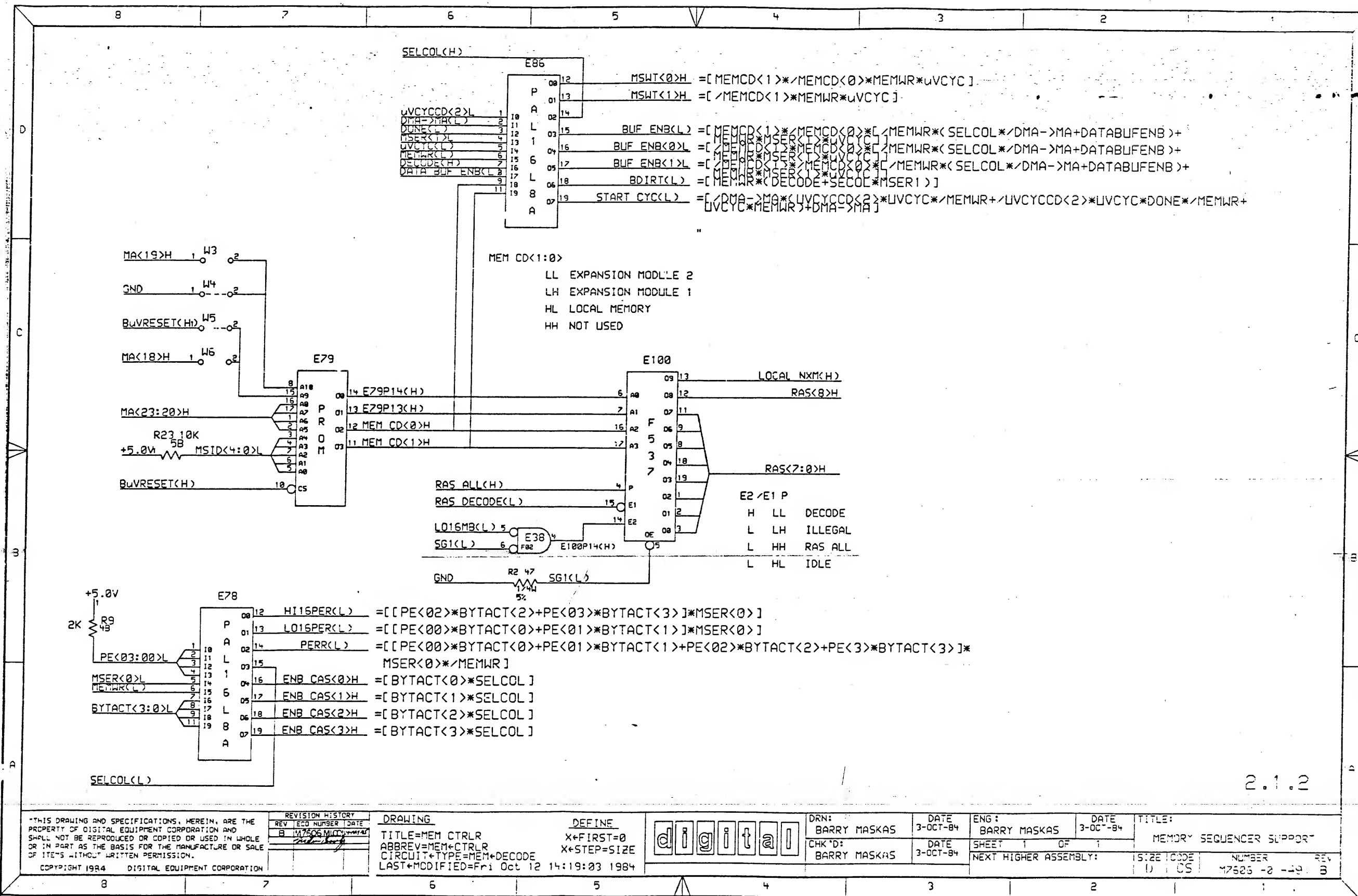
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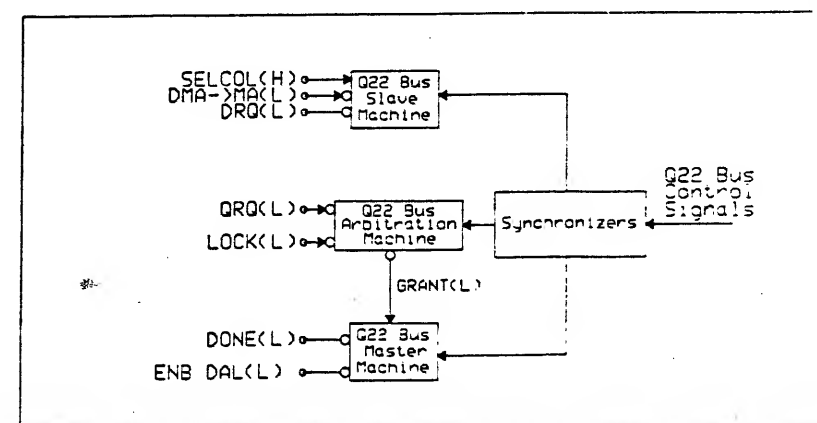
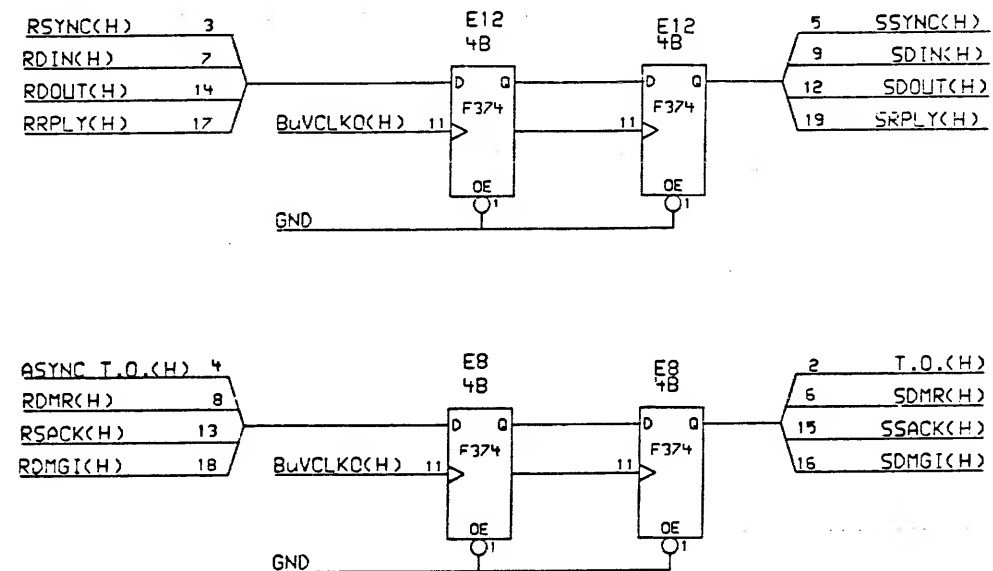
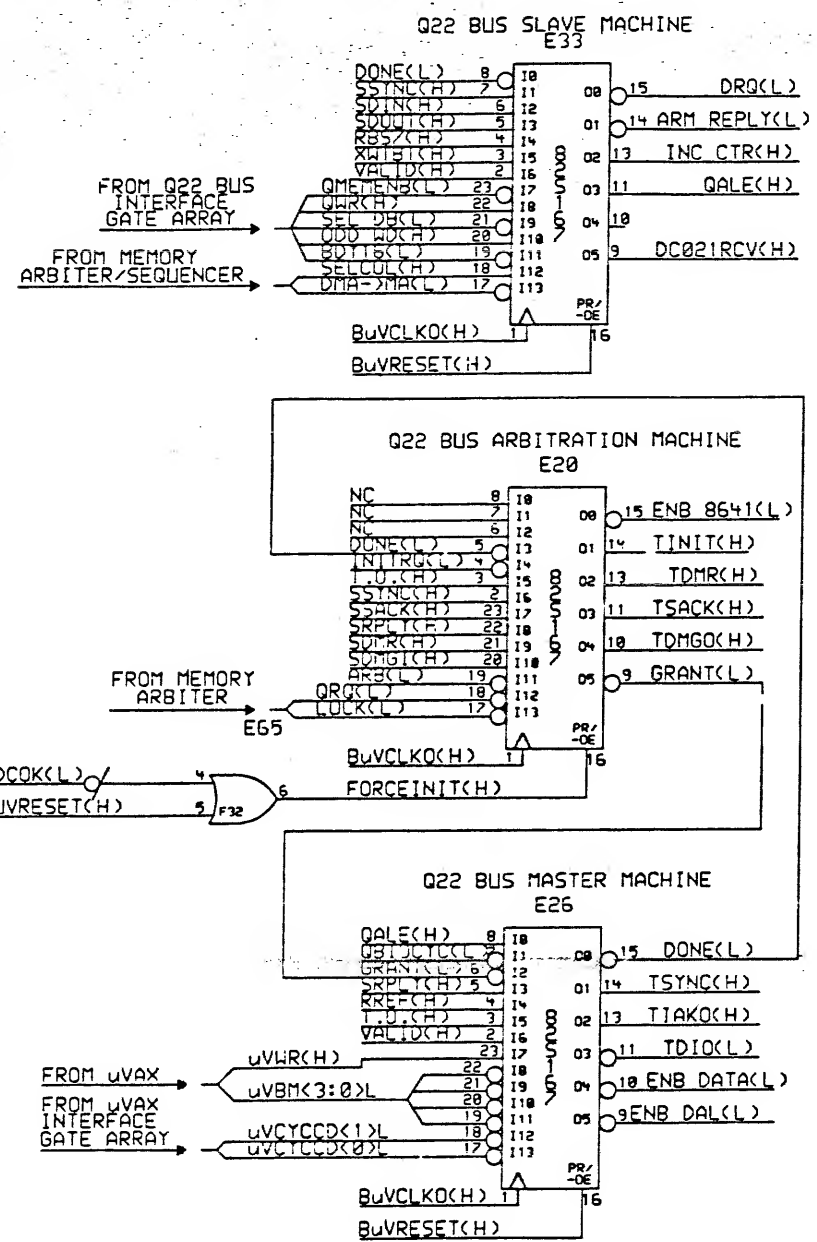
DATE 18-DEC-83

TITLE: MEMORY SEQUENCER

SIZE D CODE CS NUMBER M7635 -R -43 DEV B

2.1.1





NAME 23_053L1_00__E27 ;MEMORY ARBITER MACHINE
 OPTION PRESET
 INPUT -EPRDY, -ENBADR, -DONE, -DRQ, -CYCD0, -CYCD1, -CYCD2,
 INPUT -MEMWR, S0, S1, RR, -VCYC, -LPERR, LOCALNXM, BVAS, -VERR
 OUTPUT -DALMA, -RDYERR, -LOCK, -GRQ, DECODE, -ARMDAL, -REFMA, -DMAMA

LOCAL FLAG ;LOCK FLAG PREVENTS VAX FROM CHANGING MEMORY UNTIL Q22 BUS
 ;MASTERSHIP, Q22 BUS AND REFRESH CYCLES ARE ALLOWED.
 MACHINE 23_053L1_00__E27

STATE POWERUP ;LET REFRESH OR Q22 SLAVE THROUGH UNTIL Q22 BUS OWNED.
 IF [-DONE * S1 * -S0 * RR] THEN FINISHUP [-DMAMA, -DALMA, -DECODE,&
 -ARMDAL, -FLAG]
 IF [-DONE * DRQ] THEN FINISHUP [-DMAMA, -DALMA, -DECODE,&
 -ARMDAL, -FLAG]
 IF [DONE * -ENBADR * CYCD0] THEN VXT12 [RDYERR, ARMDAL] ;LOCAL MISS.
 IF [DONE * ENBADR * CYCD0] THEN Q22MT3 [-DALMA] ;LOCAL MISS AND GLOBAL HIT
 IF [DONE * CYCD1 * -CYCD0] THEN VXT12 [RDYERR] ;FINISH UP THE MAP CYCLE.

STATE SYNCUP, NUMBER -LLLLH
 GOTO FINISHUP [-DMAMA, -DALMA, -DECODE, -ARMDAL]

STATE FINISHUP, NUMBER -HLLH ;Q22 SLAVE CYCLES HAVE TOP PRIORITY, REFRESH
 IF [-LPERR * DRQ] THEN Q22SLAVE [DMAMA]
 IF [-LPERR * RR * -DRQ] THEN REFRESH [REFMA] ;LPERR IS FOR OPTIMIZATION.
 IF [FLAG * -RR * -DRQ] THEN VXT10 ;IF FLAGWAIT FOR DONE.
 IF [-S1 * -S0 * -EPRDY * -FLAG * -RR * -DRQ] THEN VXSLAVE [DALMA]

STATE REFRESH, NUMBER -HHHLH
 GOTO RT2

STATE RT2, NUMBER -LLLLL
 GOTO RT3

STATE RT3 ;WHEN REFRESH, RAS(8:0)H AND LOCALNXM(H) ASSERT.
 GOTO RT4

STATE RT4
 GOTO RT5 [-RDYERR]

STATE RT5
 GOTO RT6 [-REFMA]

STATE RT6
 GOTO SYNCUP [-DECODE, -RDYERR]

STATE Q22SLAVE, NUMBER -HLLH ;LOCAL MEMORY IS SLAVE TO Q22 BUS MASTER.
 GOTO RT2 [DECODE]

STATE VXSLAVE, NUMBER -HLLH ;LOCAL MEMORY IS SLAVE TO VAX.
 GOTO VXT3 [DECODE]

STATE VXT3, NUMBER -LHLL
 IF [S1 * -S0 * VCYC * BVAS * CYCD2 * -DONE] THEN READY [ARMDAL, RDYERR]
 IF [S1 * -S0 * VCYC * BVAS * -CYCD2 * -CYCD1 * -CYCD0 * DONE] THEN READY &
 [ARMDAL, RDYERR]
 IF [S1 * -S0 * VCYC * CYCD1 * CYCD0 * DONE * EPRDY] THEN READY [ARMDAL, &
 RDYERR]
 IF [S1 * -S0 * -BVAS * -VCYC] THEN FINISHUP [-DMAMA, -DALMA, &
 -DECODE, -ARMDAL] ;IF NOTHING TO DO GO LOOK FOR REFRESH OR Q22 SLAVE.
 IF [S1 * -S0 * VCYC * BVAS * -CYCD2 * -DONE] THEN RT4 [GRQ, LOCK, FLAG]
 IF [S1 * -S0 * -VCYC * BVAS] THEN VXT41 [-DECODE] ;WHAT CYCLE TO DO?

STATE VXT41 ;FIND OUT WHAT KIND OF CYCLE TO RUN?
 IF [-VCYC * CYCD2 * -CYCD1 * CYCD0] THEN Q22CYC [GRQ, -DALMA, ARMDAL]
 IF [-VCYC * -CYCD2 * -CYCD1 * CYCD0] THEN PROMCYC [RDYERR]
 IF [-VCYC * -CYCD1 * -CYCD0] THEN RT4
 IF [-VCYC * CYCD2 * CYCD1 * -CYCD0] THEN Q22CYC
 IF [-VCYC * -CYCD2 * CYCD1 * -CYCD0] THEN Q22CYC [LOCK]
 IF [-VCYC * CYCD2 * CYCD1 * CYCD0] THEN Q22CYC [ARMDAL]
 IF [-VCYC * -CYCD2 * CYCD1 * CYCD0] THEN Q22CYC [LOCK, ARMDAL]

STATE READY ;CYCLE IS RUNNING AND EPR MACHINE ASSERTS EPRDY
 IF [-S1 * S0] THEN VXT6 ;TO STROBE MEMCD(1:0) OR MSER WRITE DATA.

STATE VXT6 ;IF VAX ERROR PIN IS ASSERTED, EXTRA uCYCLE OCCURS.
 IF [VERR] THEN VXT9 [-LOCK, -GRQ] ;FREE Q22 BUS ON ERRORS OR MEMORY WRITES.
 IF [-VERR * -MEMWR] THEN VXT7 [-GRQ, -DECODE, -RDYERR, -FLAG]
 IF [-VERR * MEMWR] THEN VXT7 [-LOCK, -DECODE, -RDYERR, -FLAG, -GRQ]

STATE VXT7, NUMBER -LLLH
 GOTO VXT8 [-DMAMA, -DECODE, -DALMA, -ARMDAL]

STATE VXT8, NUMBER -HLLH ;IF LOCAL PARITY ERROR THEN PROTECT MEMORY AND WAIT
 IF [LPERR] THEN VXTHOLD [-LOCK]
 IF [-LPERR * -RR * -DRQ] THEN VXSLAVE [DALMA] ;ALLOW Q22 IAKS.
 IF [-LPERR * RR * -DRQ] THEN REFRESH [REFMA] ;ALLOW REFRESH.
 IF [-LPERR * DRQ] THEN Q22SLAVE [DMAMA] ;ALLOW Q22 SLAVE.

STATE VXTHOLD ;FORCE VAX MACHINE CHECK, THEN ALLOW MEMORY CYCLES
 IF [BVAS * S1 * -S0 * -VERR] THEN VXT9

STATE VXT9 ;STALL ONE MICROCYCLE IF VAX SAW AN ERROR.
 IF [S1 * S0 * -LOCALNXM] THEN VXT7 [-DECODE, -RDYERR]
 IF [S1 * S0 * LOCALNXM] THEN RT3 [-DECODE, -GRQ, -RDYERR, -ARMDAL]

STATE VXT10 ;STALL UNTIL Q22 BUS MASTERSHIP THEN RUN READ LOCK CYCLE.
 IF [S1 * -S0 * DONE * BVAS * -CYCD2 * -CYCD1 * -CYCD0] THEN FINISHUP &
 [-FLAG]
 IF [S1 * -S0 * -DONE * BVAS * -CYCD2 * -CYCD1 * -CYCD0] THEN FINISHUP
 IF [S1 * -S0 * -DONE * -BVAS] THEN VXT8 [-FLAG, -DMAMA, -GRQ, -DALMA, &
 -ARMDAL]

STATE PROMCYC ;EPR MACHINE RUNS A PROM CYCLE WHEN RDYERR IS ASSERTED.
 IF [EPRDY] THEN RT4 ;EPR MACHINE ASSERTS EPRDY WHEN PROM CYCLE IS DONE.

STATE VXT12 ;EPR MACHINE IS DOING THE SYNCING.
 IF [EPRDY] THEN READY [RDYERR] ;EPR MACHINE IS DONE AND VAX
 ;IS FINISHING.

STATE Q22CYC ;Q22 BUS DATA CYCLE OR IAK.
 IF [S1 * S0] THEN POWERUP [GRQ]

STATE Q22MT3 ;GET IN STEP AND GO RUN THE MISS-HIT CYCLE, TELL EPR MACHINE.
 IF [S1 * -S0] THEN Q22MT4 [DMAMA, RDYERR]

STATE Q22MT4, NUMBER -HLLH
 GOTO VXSLAVE

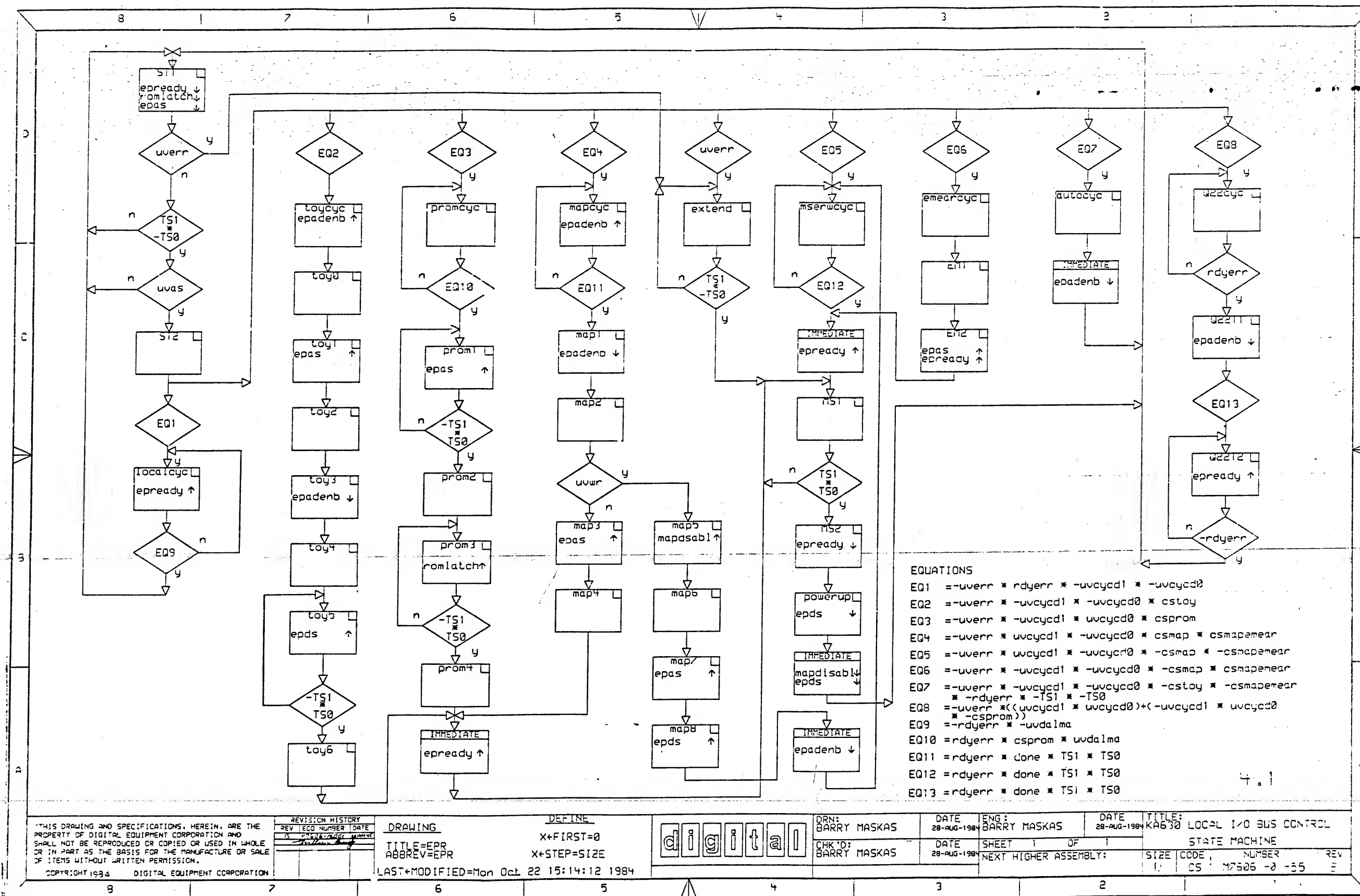
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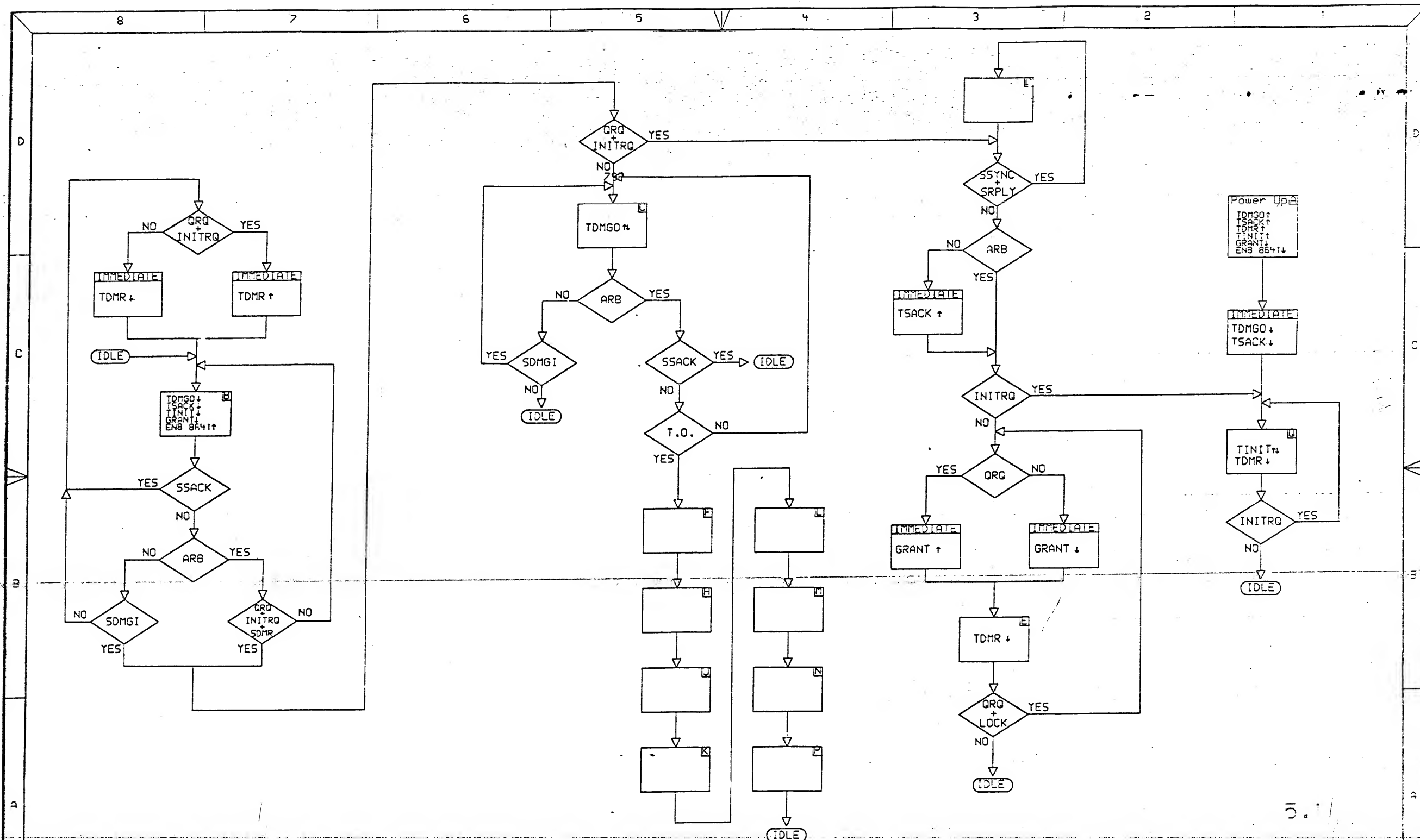
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REVISIONS
 CHK CHANGE NO. REV

digital	DATE	ENG.	DATE	TITLE
	09-AUG-95	R. MCNAMARA	09-AUG-95	MEMORY ARBITER LISTING
CHK'D	DATE	BOARD LOCATION	SIZE	CODE
R. MCNAMARA	09-AUG-95	SHEET	D	CS
FIRST USED ON OPTION/MODEL:			NUMBER	REV.
			M7606-0-51	A

8	7	6	5	4	3	2	1
<div>NAME 23_014L3_00 ;KA630 LOCAL I/O CONTROL MACHINE revision 2 OPTION PRESET INPUT NC1, -UVDALMA, -RDYERR, CSTOY, -CSPROM, -CSMAP, CSMAPMEAR, INPUT -UVCYCD0, -UVCYCD1, NC0, UVWR, -DONE, -UVERR, TS0, TS1, BUVAS OUTPUT NC3, MAPDISABLE, EPDS, -EPAS, NC2, -HIROMDLATCH, -EPADENB, -EPREADY MACHINE 23_014L3_00 STATE POWERUP GOTO ST1 [-MAPDISABLE, -EPDS, -EPREADY, -EPAS, -HIROMDLATCH] STATE ST1, NUMBER LLHLL IF [TS1 * -TS0 * BUVAS * -UVERR] THEN ST2 IF [TS1 * -TS0 * UVERR] THEN EXTEND STATE ST2, NUMBER LLLHLL ;WHAT SHOULD RUN? IF Q22 BUS PUT ADDRESS ON EPR. IF [-UVERR * RDYERR * -UVCYCD1 * -UVCYCD0] THEN LOCALCYC [EPREADY] IF [-UVERR * -UVCYCD1 * -UVCYCD0 * CSTOY] THEN TOYCYC [EPADENB] IF [-UVERR * -UVCYCD1 * UVCYCD0 * CSPROM] THEN PROMCYC IF [-UVERR * UVCYCD1 * -UVCYCD0 * CSMAP * CSMAPMEAR] THEN MAPCYC [EPADENB] IF [-UVERR * UVCYCD1 * -UVCYCD0 * -CSMAP * -CSMAPMEAR] THEN MSERWCYC IF [-UVERR * -UVCYCD1 * -UVCYCD0 * -CSMAP * CSMAPMEAR] THEN EMEARCYC IF [-UVERR * -UVCYCD1 * -UVCYCD0 * -CSTOY * -CSMAPMEAR * -RDYERR * -TS1 * & -TS0] THEN AUTOCYC IF [-UVERR * (-UVCYCD1 * UVCYCD0) + (-UVCYCD1 * UVCYCD0 * -CSPROM)] THEN Q22CYC [EPADENB] IF [UVERR] THEN EXTEND STATE EXTEND, NUMBER LLHLL IF [TS1 * -TS0] THEN MS1 STATE LOCALCYC ;FAST READY FLEW BY BUT EPREADY ASSERTS TO STROBE ERRORS. IF [-RDYERR * -UVDALMA] THEN ST1 [-EPREADY, -HIROMDLATCH, -EPAS] STATE TOYCYC, NUMBER HLLHH ;TOY CLOCK CYCLE GOTO TOYT0 STATE TOYT0, NUMBER HLLHL ;ADDRESS SETUP TIME GOTO TOYT1 [EPAS] ;CHIP SELECT AND ADDRESS ARE STABLE SO GO TO IT. STATE TOYT1, NUMBER HLLHL GOTO TOYT2 ;ADDRESS HOLD TIME. STATE TOYT2, NUMBER HLLHL GOTO TOYT3 [-EPADENB] STATE TOYT3, NUMBER HLLHL GOTO TOYT4 ;PREVENT TRISTATE OVERLAP. STATE TOYT4, NUMBER HLLHL GOTO TOYT5 [EPDS] ;GET OR PUT THE DATA. STATE TOYT5, NUMBER LLLHL ;DELAY FOR DATA ACCESS TIME. IF [-TS1 * TS0] THEN TOYT6 STATE TOYT6, NUMBER LLLHL ;TELL UVAX THAT CYCLE CAN FINISH. GOTO MS1 [EPREADY] STATE PROMCYC ;PROM CYCLE IF [UVDALMA * CSPROM * RDYERR] THEN PROMT1 [EPAS] ;ADDRESS OK? STATE PROMT1 ;DELAY FOR ACCESS TIME. IF [-TS1 * TS0] THEN PROMT2 STATE PROMT2 ;DELAY FOR ACCESS TIME, STROBE HI 16 BITS INTO LATCH. GOTO PROMT3 [HIROMDLATCH] ;CHANGE ADDRESS TO LO 16 BITS. STATE PROMT3 ;DELAY FOR ACCESS TIME. IF [-TS1 * TS0] THEN PROMT4 STATE PROMT4, NUMBER HLLHL ;TELL MEMORY MACHINE AND UVAX TO FINISH. GOTO MS1 [EPREADY] STATE MAPCYC ;MAP CYCLE IF [RDYERR * DONE * TS1 * TS0] THEN MAPT1 [-EPADENB] ;HAVE THE Q22 BUS? STATE MAPT1, NUMBER LLLHH GOTO MAPT2 ;PREVENT TRISTATE OVERLAP. STATE MAPT2, NUMBER LLLHL ;READ OR WRITE CYCLE? IF [UVWR] THEN MAPT5 [MAPDISABLE] ;IF WRITE THEN 2 THE MAP OUTPUTS. IF [-UVWR] THEN MAPT3 [EPAS] ;IF READ THEN GET DATA ON EPR BUS. STATE MAPT3, NUMBER HLLHL GOTO MAPT4 ;DELAY ONE TICK TO SYNC UP. STATE MAPT4, NUMBER HLLHL ;TELL UVAX AND MEMORY MACHINE TO FINISH. GOTO MS1 [EPREADY] STATE MAPT5 GOTO MAPT6 ;PREVENT TRISTATE OVERLAP. STATE MAPT6 ;ENABLE THE WRITE DATA. GOTO MAPT7 [EPAS] STATE MAPT7 ;ASSERT THE WRITE STROBE. GOTO MAPT8 [EPDS] STATE MAPT8 ;SYNC UP WITH UVAX AND MEMORY MACHINE. GOTO MSERWCYC [-EPADENB] STATE MSERWCYC ;MSER WRITE CYCLE, GET THE Q22 BUS, STROBE THE DATA. IF [RDYERR * DONE * TS1 * TS0] THEN MS1 [EPREADY] STATE MS1, NUMBER LLLHL ;STROBE THE MSER DATA WITH EPREADY. IF [TS1 * TS0] THEN MS2 [-EPREADY] STATE MS2 GOTO POWERUP [-EPDS] STATE EMEARCYC, NUMBER HLLHL ;EXTERNAL MEAR CYCLE. GOTO EM1 STATE EM1, NUMBER HLLHL ;ENABLE THE EPR DATA AND TELL UVAX TO FINISH. GOTO EM2 [EPAS, EPREADY] STATE EM2, NUMBER HLLHL GOTO MS1 [EPREADY] STATE AUTOCYC ;NOTHING TO DO SO BACK FOR ANOTHER LOOK. GOTO ST1 [-EPREADY, -HIROMDLATCH, -EPAS, -EPADENB] STATE Q22CYC ;Q22 BUS [AK OR Q22 BUS READ OR WRITE. IF [RDYERR] THEN Q22T1 [-EPADENB] STATE Q22T1 IF [RDYERR * DONE * TS1 * TS0] THEN Q22T2 [EPREADY] STATE Q22T2 ;WAIT UNTIL MEMORY MACHINE IS DONE. IF [-RDYERR] THEN ST1 [-EPREADY, -HIROMDLATCH, -EPAS] END</div>							





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REVISION HISTORY		
REV	ECO NUMBER	DATE
1	1	6-7-84

DRAWING
TITLE=ARB
ABBREV=arb

LAST MODIFIED=Mon Oct 22 15:04:38 1984

DEFINE

X+FIRST=0
X+STEP=SIZE

digital

DRN:
R. McNamara
CHK'D:
R. McNamara

DATE
6-Jul-84
DATE
6-Jul-84

ENG:
R. McNamara
SHEET
1 OF 1
NEXT HIGHER ASSEMBLY:

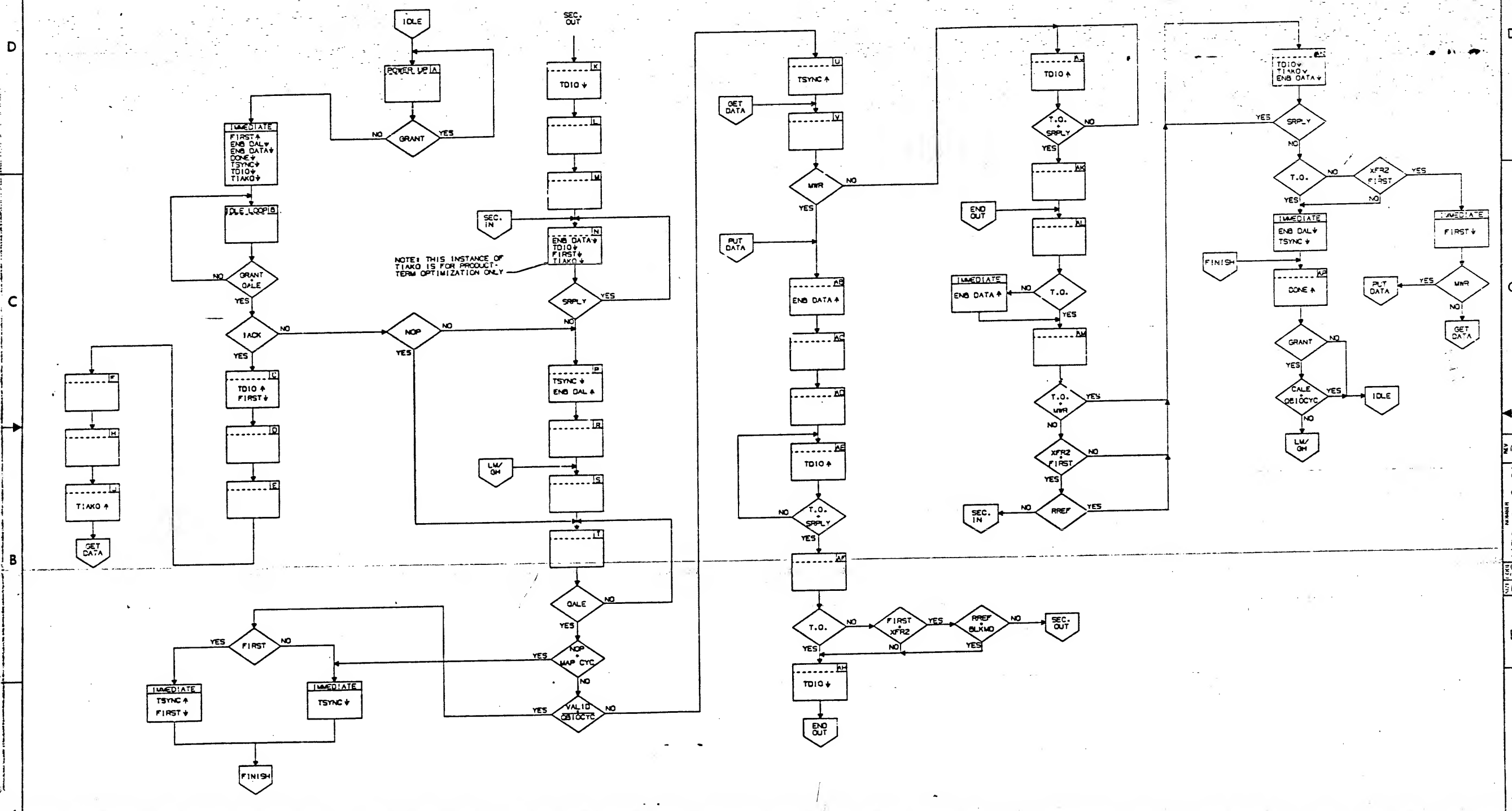
DATE
6-Jul-84

TITLE:
QBUS ARBITRATION CONTROL
DETAILED CONTROL FLOW DIAGRAM

SIZE CODE NUMBER
D 05 M7525 -2 -57

8	7	6	5	4	3	2	1
<div>name 23_009L3_00_E26 ;Q22 bus master cycle control machine</div> <div>input nci15, -cd0, -cd1, -bm0, -bm1, -bm2, -bm3, uVWR</div> <div>input valid, nci16, t_o, rref, srply, -grant, -qblocyc, qale</div> <div>output nco7, -EnbDal, -EnbData, -tdio, nco3, tiako, tsync, -done</div> <div>local first</div> <div>machine q_bus_master</div> <div>state A, number -hhhhh</div> <div>if [-grant] then B [first, -EnbDal, -EnbData, -done, -tdio, -tiako, -tsync]</div> <div>state B, number -hhhlh</div> <div>if [grant * qale * (-cd1)] then P [EnbDal]</div> <div>if [grant * qale * (-cd1 * -cd0)] then I</div> <div>if [grant * qale * (-cd1 * cd0)] then C [tdio, -first]</div> <div>state C, number -hlhlh</div> <div>goto D</div> <div>state D, number -llhlh</div> <div>goto E</div> <div>state E, number -hlhjh</div> <div>goto F</div> <div>state F, number -lllhj</div> <div>goto H</div> <div>state H, number -hlhjh</div> <div>goto J [tiako]</div> <div>state J, number -lhhlh</div> <div>goto V</div> <div>state K, number -hlhjh</div> <div>goto L</div> <div>state L, number -hhhlh</div> <div>goto M</div> <div>state M, number -lhhlh</div> <div>goto N [-EnbData, -tdio, -first]</div> <div>state N, number -lhhlh</div> <div>if [-srply] then P [EnbDal, -tsync]</div> <div>state P, number -hlhlh</div> <div>goto R</div> <div>state R, number -llhlh</div> <div>goto S</div> <div>state S, number -hlhjh</div> <div>goto T</div> <div>state T, number -llhjh</div> <div>if [qale * (-cd0 + (valid * qblocyc))] &</div> <div>then AP [done]</div> <div>if [qale * cd0 * (-valid + qblocyc)] &</div> <div>then U [tsync]</div> <div>if [qale * cd0 * valid * -qblocyc * -first] then [-tsync]</div> <div>if [qale * cd0 * valid * -qblocyc * first] then [tsync, -first]</div> <div>state U, number -hlhlh</div> <div>goto V</div> <div>state V, number -llhlh</div> <div>if [uVWR] then AB [EnbData]</div> <div>if [-uVWR] then AJ [tdio, -EnbDal]</div> <div>state AJ, number -hhhlh</div> <div>if [t_o + srply] then AK</div> <div>state AK, number -hlhlh</div> <div>goto AL</div> <div>state AL, number -lllhj</div> <div>goto AM</div> <div>if [-t_o] then [EnbData]</div> <div>state AM, number -hlhlh</div> <div>if [-t_o * -uVWR * (bm2*bm1) * first * -rref] then N &</div> <div>[-EnbData, -tdio, -tiako, -first]</div> <div>if [t_o + uVWR + -(bm2*bm1) + -first + rref] then AN &</div> <div>[-EnbData, -tdio, -tiako]</div> <div>state AN, number -lllhj</div> <div>if [-srply * -t_o * first * (bm2*bm1) * -uVWR] &</div> <div>then V [-first]</div> <div>if [-srply * -t_o * first * (bm2*bm1) * uVWR] &</div> <div>then AB [-first, EnbData]</div> <div>if [-srply * (t_o + -(bm2*bm1) + -first)] &</div> <div>then AP [-tsync, done, -EnbDal]</div> <div>state AP, number -hlhjh</div> <div>if [grant * -qblocyc * -qale] then S</div> <div>if [-grant + qblocyc + qale] then A</div> <div>state AB, number -hhhlh</div> <div>goto AC</div> <div>state AC, number -lhhlh</div> <div>goto AD</div> <div>state AD, number -hhhlh</div> <div>goto AE [tdio]</div> <div>state AE, number -hhhlh</div> <div>if [t_o + srply] then AF</div> <div>state AF, number -hlhlh</div> <div>if &</div> <div>[-t_o * first * (bm2*bm1) * -(uVWR + bm0 * bm3) * rref]] &</div> <div>then K [-tdio]</div> <div>if &</div> <div>[t_o + -first + -(bm2*bm1) + rref * (-uVWR + bm0 * bm3)] &</div> <div>then AH [-tdio]</div> <div>state AH, number -llhlh</div> <div>goto AL</div> <div>END</div>							
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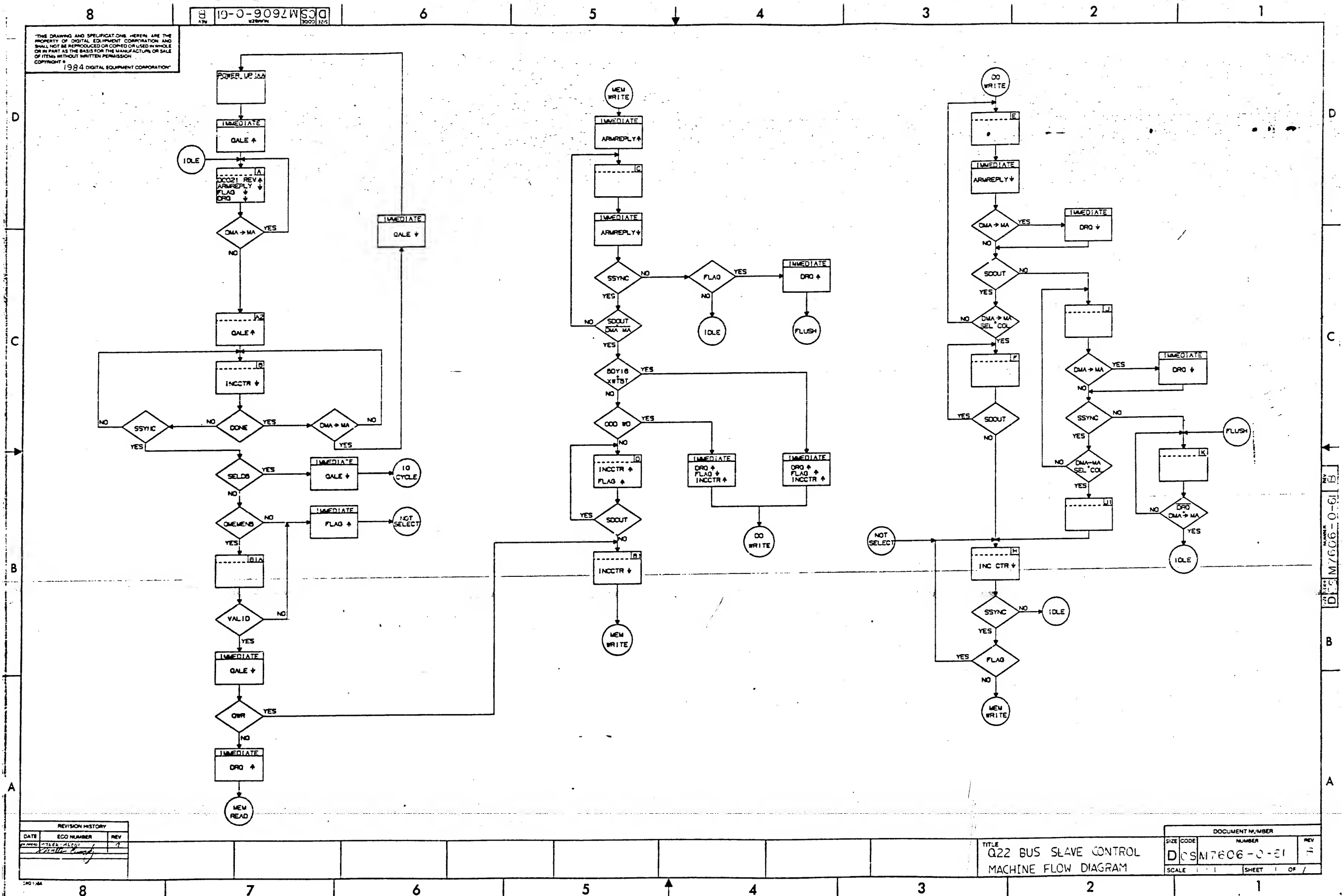


REVISION HISTORY		
DATE	ECO NUMBER	REV
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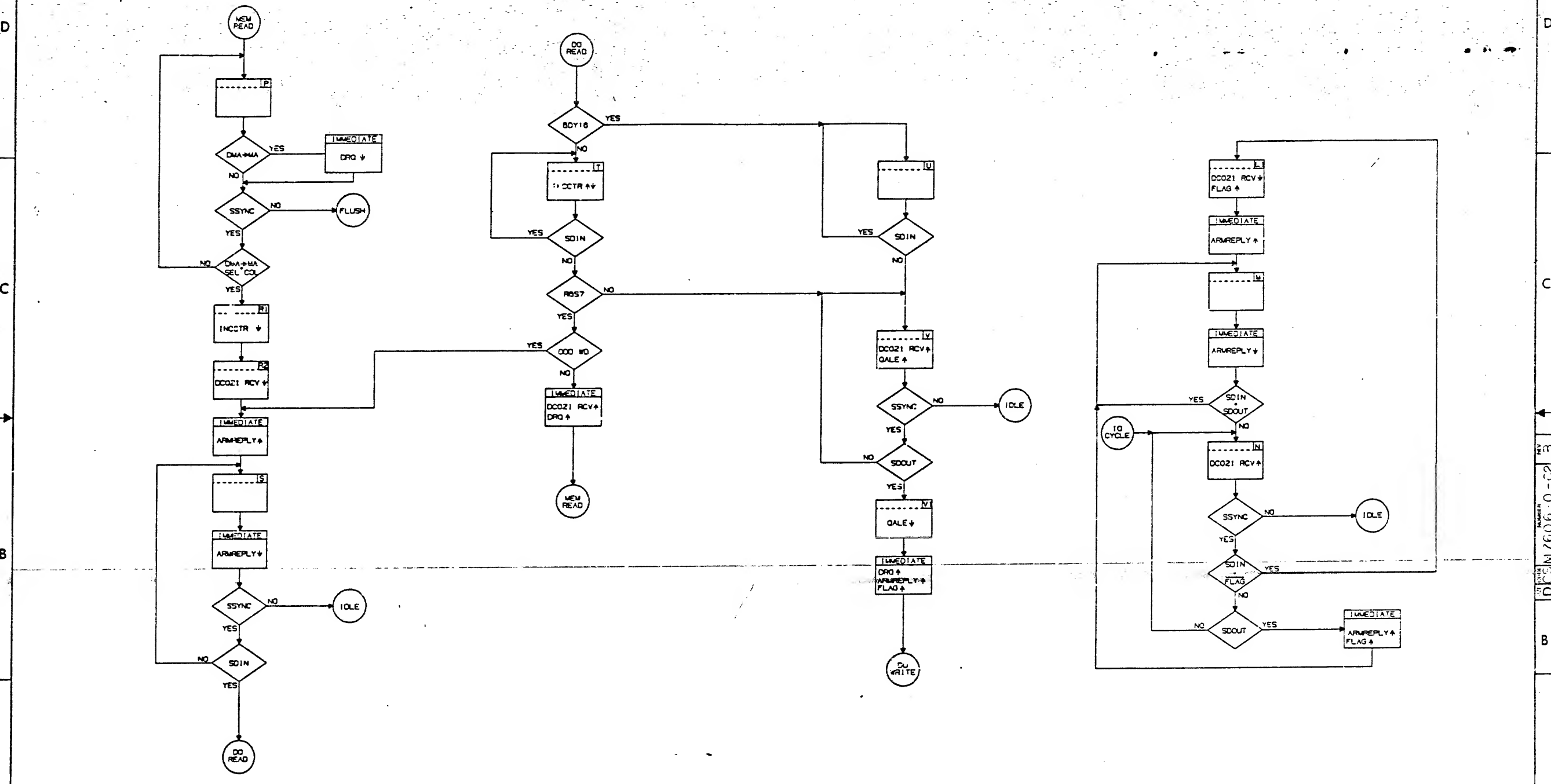
TITLE
Q22 BUS MASTER CONTROL
MACHINE FLOW DIAGRAM

DOCUMENT NUMBER		
SIZE	NUMBER	REV
D	CS M7606-0-59	3
SCALE	SHEET	OF

8	7	6	5	4	3	2	1
						REV. A	SIZE CODE D CS 3000 3215
<div>name 22_010L3_00_E33 ;Q22 bus slave cycle control machine</div> <div>input -drq, -dmaMA, selcol, -bdy16, oddwd, -sel_db, qwr, -QMemEnb</div> <div>valid, nci6, xwtbt, rbs7, sdout, sdin, ssync, -done</div> <div>output nco7, DC021rcv, nco5, qale, nco3, incctr, -armreply, -drq</div> <div>local flag</div> <div>machine q_bus_slave</div> <div>state AA, number -hhhhh</div> <div>goto A [DC021rcv, -drq, qale, -armreply, -flag]</div> <div>state A, number -11111</div> <div>if [-dmaMA] then A2 [qale]</div> <div>state A2, number -1h111</div> <div>goto B [-incctr]</div> <div>state B1, number -1hh11</div> <div>goto C [armreply]</div> <div>state C, number -1h111</div> <div>always [-armreply]</div> <div>if [-ssync * flag] then K [drq]</div> <div>if [-ssync * -flag] then A &</div> <div>[DC021rcv, -armreply, -flag, -drq]</div> <div>if [ssync * sdout * -dmaMA * -xwtbt * -bdy16 * -oddwd] then D [incctr, flag]</div> <div>if [ssync * sdout * -dmaMA * (xwtbt + bdy16)] then E [drq, flag, incctr]</div> <div>if [ssync * sdout * -dmaMA * -xwtbt * -bdy16 * oddwd] then E &</div> <div>[drq, -flag, incctr]</div> <div>state D</div> <div>if [-sdout] then B1 [-incctr]</div> <div>state E, number -1h11h</div> <div>always [-armreply]</div> <div>if [dmaMA] then [-drq]</div> <div>if [-sdout] then J</div> <div>if [sdout * dmaMA * selcol] then F</div> <div>state F</div> <div>if [-sdout] then H [-incctr]</div> <div>state H, number -1h11h</div> <div>if [-ssync] then A [DC021rcv, -armreply, -flag, -drq]</div> <div>if [ssync * -flag] then C [armreply]</div> <div>state J, number -h111h</div> <div>if [dmaMA] then [-drq]</div> <div>if [-ssync] then K</div> <div>if [ssync * dmaMA * selcol] then J1</div> <div>state J1, number -hh11h</div> <div>goto H [-incctr]</div> <div>state K, number -1111h</div> <div>if [dmaMA * -drq] then A [DC021rcv, -armreply, -flag, -drq]</div> <div>state L1, number -1hhhh</div> <div>goto M [armreply]</div> <div>state M, number -11hhh</div> <div>always [-armreply]</div> <div>if [-sdin * -sdout] then N [DC021rcv]</div> <div>state N, number -11111</div> <div>if [-ssync] then A [DC021rcv, -armreply, -flag, -drq]</div> <div>if [ssync * sdin * -flag] then L1 [-DC021rcv, flag]</div> <div>if [ssync * -(sdin * -flag) * sdout] then M [armreply, flag]</div> <div>state P, number -h1111</div> <div>if [dmaMA] then [-drq]</div> <div>if [-ssync] then K</div> <div>if [ssync * dmaMA * selcol] then R</div> <div>state R, number -hh111</div> <div>goto R1 [-incctr]</div> <div>state R1, number -hh1h1</div> <div>goto R2 [-DC021rcv]</div> <div>state R2, number -1hhhl</div> <div>goto S [armreply]</div> <div>state S, number -11hh1</div> <div>always [-armreply]</div> <div>if [-ssync] then A [DC021rcv, -armreply, -flag, -drq]</div> <div>if [ssync * sdin * bdy16] then U</div> <div>if [ssync * sdin * -bdy16] then T [incctr]</div> <div>state T</div> <div>if [-sdin * -rbs7] then V &</div> <div>[-incctr, DC021rcv, qale]</div> <div>if [-sdin * rbs7 * oddwd] then S &</div> <div>[-incctr, armreply]</div> <div>if [-sdin * rbs7 * -oddwd] then P &</div> <div>[-incctr, DC021rcv, drq]</div> <div>state U</div> <div>if [-sdin] then V [DC021rcv, qale]</div> <div>state V, number -h11h1</div> <div>if [-ssync] then A [DC021rcv, -armreply, -flag, -drq]</div> <div>if [ssync * sdout] then V1 [-qale]</div> <div>state V1, number -1hh1h</div> <div>goto E [armreply, flag, drq]</div> <div>state B, number -1h1h1</div> <div>if [-done * ssync * -sel_db * QMemEnb] then B1A</div> <div>if [-done * ssync * -sel_db * -QMemEnb] then H [flag, -incctr]</div> <div>if [-done * ssync * sel_db] then N [-qale, DC021rcv]</div> <div>if [done * dmaMA] then AA [-qale]</div> <div>state B1A</div> <div>if [-valid] then H [flag, -incctr]</div> <div>if [valid * -qwr] then P [-qale, drq]</div> <div>if [valid * qwr] then B1 [-qale, -incctr]</div> <div>END</div>							
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8	7	6	5	4	3	2	1



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REVISION HISTORY		
DATE	ECO NUMBER	REV

TITLE
322 BUS SLAVE CONTROL
MACHINE FLOW DIAGRAM

DOCUMENT NUMBER		
SIZE	CODE	NUMBER
D	CS	M7606-0-62
SCALE	SHEET	OF

8	7	6	5	4	3	2	1									
<div> <div>DEC PART NUMBER: 23-E42F1-00 KA630 -A, -B 1MB RAS DECODE PROM (E79)</div> <div>DATE ORIGINATED: 10-September-1984</div> </div>																
<div>HEX LOC DATA</div> <div>000 9</div> <div>001 9</div> <div>002 9</div> <div>003 9</div> <div>004 9</div> <div>005 9</div> <div>006 9</div> <div>007 9</div> <div>008 9</div> <div>009 9</div> <div>00A 9</div> <div>00B 9</div> <div>00C 9</div> <div>00D 9</div> <div>00E 9</div> <div>00F 9</div> <div>010 9</div> <div>011 9</div> <div>012 9</div> <div>013 9</div> <div>014 9</div> <div>015 9</div> <div>016 9</div> <div>017 9</div> <div>018 9</div> <div>019 9</div> <div>01A 9</div> <div>01B 9</div> <div>01C 9</div> <div>01D 9</div> <div>01E 9</div> <div>01F 9</div> <div>020 9</div> <div>021 9</div> <div>022 9</div> <div>023 9</div> <div>024 9</div> <div>025 9</div> <div>026 9</div> <div>027 9</div> <div>028 9</div> <div>029 9</div> <div>02A 9</div> <div>02B 9</div> <div>02C 9</div> <div>02D 9</div> <div>02E 9</div> <div>02F 9</div> <div>030 9</div> <div>031 9</div> <div>032 9</div> <div>033 9</div> <div>034 9</div> <div>035 9</div> <div>036 9</div> <div>037 9</div> <div>038 9</div> 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<div>367 9</div> <div>368 9</div> <div>369 9</div> <div>36A 9</div> <div>36B 9</div> <div>36C 9</div> <div>36D 9</div> <div>36E 9</div> <div>36F 9</div> <div>370 9</div> <div>371 9</div> <div>372 9</div> <div>373 9</div> <div>374 9</div> <div>375 9</div> <div>376 9</div> <div>377 9</div> <div>378 9</div> <div>379 9</div> <div>37A 9</div> <div>37B 9</div> <div>37C 9</div> <div>37D 9</div> <div>37E 9</div> <div>37F 9</div> <div>380 9</div> <div>381 9</div> <div>382 9</div> <div>383 9</div> <div>384 9</div> <div>385 9</div> <div>386 9</div> <div>387 9</div> <div>388 9</div> <div>389 9</div> <div>38A 9</div> <div>38B 9</div> <div>38C 9</div> <div>38D 9</div> <div>38E 9</div> <div>38F 9</div> <div>390 9</div> <div>391 9</div> <div>392 9</div>	<div>HEX LOC DATA</div> <div>393 9</div> <div>394 9</div> <div>395 9</div> <div>396 9</div> <div>397 9</div> <div>398 9</div> <div>399 9</div> <div>39A 9</div> <div>39B 9</div> <div>39C 9</div> <div>39D 9</div> <div>39E 9</div> <div>39F 9</div> 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<div>3D9 9</div> <div>3DA 9</div> <div>3DB 9</div> <div>3DC 9</div> <div>3DD 9</div> <div>3DE 9</div> <div>3DF 9</div> <div>3E0 9</div> <div>3E1 9</div> <div>3E2 9</div> <div>3E3 9</div> <div>3E4 9</div> <div>3E5 9</div> <div>3E6 9</div> <div>3E7 9</div> <div>3E8 9</div> <div>3E9 9</div> <div>3EA 9</div> <div>3EB 9</div> <div>3EC 9</div> <div>3ED 9</div> <div>3EE 9</div> <div>3EF 9</div> <div>3F0 9</div> <div>3F1 9</div> <div>3F2 9</div> <div>3F3 9</div> <div>3F4 9</div> <div>3F5 9</div> <div>3F6 9</div> <div>3F7 9</div> <div>3F8 9</div> <div>3F9 9</div> <div>3FA 9</div> <div>3FB 9</div> <div>3FC 9</div> <div>3FD 9</div> <div>3FE 9</div> <div>3FF 9</div>

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REVISIONS

CHK CHANGE NO. REV

digital

DATE 09-AUG-85

ENG. R. MCNAMARA

DATE 09-AUG-85

CHK'D R. MCNAMARA

DATE 09-AUG-85

SHEET 1 OF 1

DSK:4.12P(4,550)

09-AUG-85 02:39

NEXT HIGHER ASSEMBLY:

FIRST USED ON OPTION/MODEL:

TITLE: 1KX4 RAS DECODE PROM (E79) LISTING

SIZE CODE NUMBER REV.

D CS M7606-0-63 A

8	7	6	5	4	3	2	1
<p>T: PAL16L8A P: 23-169J5-00 E40 N: BARRY MASKAS D: 25 OCT 1984 S: /RPOK /BTRYOK CSMAPEMEAR /EPAS EPDS UVWR /DONE GALE /GRANT GND SRPLY /CLRPSH /ENBLS646 /WRMAP /ENBBDAL RDIN DC021RCV /TDIO /RCVBDALH VCC B: IF [VCC] CLRPSH = RPOK + BTRYOK IF [VCC] ENBLS646 = CSMAPEMEAR * EPAS IF [VCC] WRMAP = CSMAPEMEAR * UVWR * EPDS IF [VCC] ENBBDAL = /GRANT * /RDIN * /DONE + GRANT * /DONE * GALE + /DC021RCV * /GRANT * /DONE IF [VCC] RCVBDALH = /TDIO * /DC021RCV + /TDIO * GRANT + /SRPLY * /DC021RCV + /SRPLY * GRANT + UVWR * /DC021RCV + UVWR * GRANT E: KA630-A, -B, -C, -D (M7606) MISC. CONTROL STROBES</p> <p>T: PAL16L8A P: 23-170J5-00 E78 N: BARRY MASKAS D: 25 OCT 1984 S: /PE3 /PE2 /PE1 /PE0 /MSER0 /MEMWR /BYTACT3 /BYTACT2 /BYTACT1 GND /BYTACT0 /HI16PER /LO16PER /PERR /SELCOL /ENBCAS0H /ENBCAS1H /ENBCAS2H /ENBCAS3H VCC B: IF [VCC] HI16PER = MSER0 * PE2 * BYTACT2 + MSER0 * PE3 * BYTACT3 IF [VCC] LO16PER = MSER0 * PE0 * BYTACT0 + MSER0 * PE1 * BYTACT1 IF [VCC] PERR = MSER0 * /MEMWR * PE0 * BYTACT0 + MSER0 * /MEMWR * PE1 * BYTACT1 + MSER0 * /MEMWR * PE2 * BYTACT2 + MSER0 * /MEMWR * PE3 * BYTACT3 IF [VCC] ENBCAS0H = /SELCOL + /BYTACT0 IF [VCC] ENBCAS1H = /SELCOL + /BYTACT1 IF [VCC] ENBCAS2H = /SELCOL + /BYTACT2 IF [VCC] ENBCAS3H = /SELCOL + /BYTACT3 E: KA630-A, -B, -C, -D (M7606) MEMORY SYSTEM CAS CONTROL STROBES AND E: PARITY ERROR DETECTION STROBES</p> <p>T: PAL16L8A P: 23-171J5-00 E86 N: BARRY MASKAS D: 25 OCT 1984 S: /UVCYCCD2 /DMAMA /DONE /MSER1 /UVCYC /MEMWR DECODE /DATABUFENB MEMCD0 GND MEMCD1 /MSWT0H /MSWT1H SELCOL /BUFENB /BUFEN0 /BUFEN1 /BDIRT /STARTCYC VCC B: IF [VCC] MSWT0H = /MEMCD1 + MEMCD0 + /MEMWR + /UVCYC IF [VCC] MSWT1H = MEMCD1 + /MEMWR + /UVCYC IF [VCC] BUFENB = MEMCD1 * /MEMCD0 * /MEMWR * SELCOL * /DMAMA + MEMCD1 * /MEMCD0 * /MEMWR * DATABUFENB + MEMCD1 * /MEMCD0 * MEMWR * UVCYC * MSER1 IF [VCC] BUFEN0 = /MEMCD1 * /MEMCD0 * /MEMWR * SELCOL * /DMAMA + MEMCD1 * /MEMCD0 * /MEMWR * DATABUFENB + /MEMCD1 * MEMCD0 * MEMWR * UVCYC * MSER1 IF [VCC] BUFEN1 = /MEMCD1 * /MEMCD0 * /MEMWR * SELCOL * /DMAMA + MEMCD1 * /MEMCD0 * /MEMWR * DATABUFENB + /MEMCD1 * MEMCD0 * MEMWR * UVCYC * MSER1 IF [VCC] BDIRT = MEMWR * DECODE + MEMWR * SELCOL * MSER1 IF [VCC] STARTCYC = /DMAMA * UVCYCCD2 * UVCYC * /MEMWR + /DMAMA * DECODE * /UVCYCCD2 * UVCYC * /MEMWR * DONE + /DMAMA * UVCYC * MEMWR * DMAMA * DECODE * DMAMA * SELCOL E: KA630-A, -B, -C, -D (M7606) MEMORY SUBSYSTEM BUFFER CONTROL STROBES E: AND MEMORY CYCLE ENABLE STROBE</p>							
8	7	6	5	4	3	2	1

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				FIRST USED ON OPTION/MODEL:		SIZE CODE D CS		NUMBER M7606-0-64		REV. A

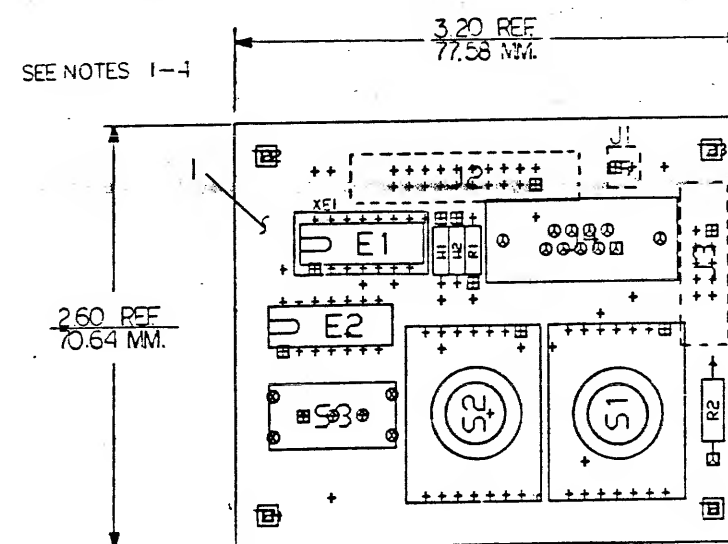
	8	7	6	5	4	3	2	1			
							0 A3B	S9-0-90924 8304M	S3 3003	D 3E1S	
	+12.0V	raw +12 volts				CS MAP;EMEAR(H)	chip select for MAP or EMEAR (external mem. err. addr. reg.)				
	+3VA	logic "high" voltage				CS PROM(L)	chip select for PROM				
	+5.0V	raw +5 volts				CS TOY(H)	chip select for TOY				
	-12.0V	charge pump generated -12 volts				CTL XDAL<1:0>H	address function bits (see table on 1.7)				
	ARB(L)	asserted if module is bus arbiter				DATA BUF ENB(L)	qbus slave memory cycle				
	ARM REPLY(L)	sets ENBREPLY (inside Qbus gate array)				DC02IRCV(H)	controls direction of DC021 during slave mode transactions				
	ARM UVDAL(L)	asserted to enable the uVDAL (->) MD transceivers				DECODE(H)	allows memory sequencer to decode and RAS memory				
	ARMRDYERR(L)	indicates that memory arbiter is READY to finish a cycle				DLAD<1:0>H	the two lo-order address lines for the DLART				
	ASYNC T.O.(H)	Q-bus timeout				DLRD(L)	read signal for DLART				
	AUX HLT(H)	auxiliary processor halt				DLRRQ(H)	receiver interrupt from DLART				
	BBS7(L)	Qbus B57 (selects I/O page, used in block mode handshake)				DSI(H)	serial data in (<to DLART)				
	BDAL<21:0>L	Qbus data/address lines				DLSO(H)	serial data out (<from DLART)				
	BDCOK(H)	Qbus DCOK signal (indicates DC power at proper level)				DLWR(L)	write signal for DLART				
	BDS CD<1:0>L	firmware mode select from configuration connector to BDR				DLXRC(H)	transmitter interrupt from DLART				
	BDIN(L)	Qbus DIN control signal				DMA->MAC(L)	"DMA acknowledge" from main memory state machine				
	BDIRT(L)	dram buffer direction transmit enable				DOK(H)	delayed indication of DC power at proper level				
	BDMGI(L)	Qbus DMGI (DMA grant in)				DONE(L)	indicates that requested transaction is completed				
	BDMGO(L)	Qbus DMGO (DMA grant out)				DRDCK(H)	delayed indication of DC power at proper level				
	BDMR(L)	Qbus DMR (DMA request)				DRQL(L)	DMA request to main memory state machine				
	BDOUL(L)	Qbus DOUT control signal				ENB 8641(L)	enable for Qbus drivers (<for disabling drivers at power up>)				
	BDR<3:0>L	boot and diagnostic register LED controls				ENB BDAL(L)	output enable for DC021 xcvr's				
	B0Y16(L)	indicates address is at a 16 word boundary				ENB CAS<3:0>H	select column and byte active controlled				
	BEVENT(L)	Qbus EVENT signal (terminated but not used)					column address strobe enables				
	BHALT(L)	Qbus HALT signal				ENB DAL(L)	enable data/address onto Q-bus				
	BIAKI(L)	Qbus IAKI (interrupt acknowledge in)				ENB DATA(L)	r/x'd output; enables data onto Q-bus (write), or strobes data in from Q-bus (read)				
	BIAKO(L)	Qbus IAKO (interrupt acknowledge out)					output enable control strobe for DPR <-> XLAT AD transceivers				
	BINIT(L)	Qbus INIT signal (clobbers/inits everybody on bus)				ENB L5646(L)	external processor bus (local I/O bus) address enable				
	BIRQ<7:4>L	Qbus IRQ lines (interrupt requests)				EPAD ENB(L)	firmware proms LSB address control				
	BMAAC<8:0>H	buffered and damped local dram array address signals				EPAC<1>H	external processor bus (local I/O bus) address strobe				
	BMCAS<3:0>H	byte active controlled unbuffered column address strobes				EPAS(L)	external processor bus (local I/O bus) data strobe				
	BMSWT<0>L	buffered and damped local dram array write signal				EPDS(H)	external processor bus (local I/O bus) address/data bus				
	BPOK(H)	Qbus POK signal (indicates sufficient power for operation)				EPR<15:0>H	auxiliary machine arm for DC379 READY or UVERR logic				
	BREAK(H)	serial line break indication from DLART				EPREADY(H)	assertion forces arbitration machine to reset and assert TINIT				
	BREF(L)	Qbus REF signal (used in block mode handshake)				FORCEINIT(H)	low 16 mega-byte normal (fast) uVAX ready strobe				
	BRPLY(L)	Qbus RPLY control signal (reply)				FSTRDY(H)	Q-bus grant sent to Q-bus Master state machine				
	BRS<2:0>L	bit rate selection (<from back panel into DLART>)				GRANT(L)	high word parity error from memory sequencer				
	BSACK(L)	Qbus SACK control signal (bus acknowledge)				H116PER(L)	signals uVAX intfc gate array to latch hi-order rom data				
	BSYNC(L)	Qbus SYNC control signal (strobes address, frames transactions)				HIROMDLATCH(L)	configuration connector buffered halt enable mask and BDR flag				
	BTRY OK(L)	indicates battery voltage above minimum threshold				HLT ENB(L)	increments block mode address counter				
	BTRYV(H)	raw battery voltage from back panel				INC CTR(H)	init request from uVAX's bus init register				
	BTRYVI(H)	battery or system voltage supply to watch/ram (TOY) chip				INTRQL(L)	interval timer 10m5				
	BTVREF(H)	battery supplied reference voltage (used to detect the battery)				INTVL TIM(L)	uVAX interrupt request inputs for processor levels 17, 16, 15				
	BUF ENB(L)	local dram array data transceiver receive direction enable				IRQ<7:5>L	indicates address is in low 16 MB of 30 bit address space				
	BUF ENB<1:0>L	expansion dram array data transceiver receive direction enable				LO16MB(L)	low word parity error from memory sequencer				
	BUVAS(H)	buffered uVAX address strobe				LO16PER(L)	low 16 megabyte non-existent physical memory flag				
	BUVAL(L)	buffered uVAX address strobe				LOCAL NXM(H)	asserted if uVAX is doing "read lock/write unlock"				
	BUVCLK(H)	buffered uVAX clock out				LOCK(L)	local dram array transceiver generated byte parity data bits				
	BUVRESET(H)	buffered uVAX reset				LPD<3:0>H	local dram array transceiver data bits				
	BUVRESET(L)	buffered uVAX reset				LRD<31:0>H	local low 16 mega-byte dram parity error strobe				
	BUTBT(L)	Qbus WBT signal (indicates write cycle, and byte write)				LPERR(L)	memory address bus				
	BYTACT<3:0>L	byte active bits to mem sequencer				MA<23:2>H	row/column multiplexed memory address bus				
	CAS<3:0>L	buffered and damped local dram array column address strobes				MAAC<9:0>L	RDAL bits 21:9 latched for translation map				
	CLK 614.4KHZ(H)	clock from 614.4KHz oscillator				MAP AD<21:9>H	scatter/gather map ram output enable control				
	CLK 614.4KHZ(L)	clock from 614.4KHz oscillator				MAP DISABLE(H)	local dram array buffered address signals				
	CLK031(H)	clock from 32KHz oscillator (31us period)				MBMAAC<8:0>H	local dram array buffered write strobe				
	CLK25(H)	clock from 40MHz oscillator (25ns period)				MBMSWT<0>L	local dram array buffered column address strobes				
	CLR PS(H)	clear power sense in TOY clock				MCAS<3:0>L	32 bit memory data bus				
	CONF<3:2>L	configuration connector buffered inputs (see table on 1.10)				MD<31:0>H	memory array selection codes (see 2.1.2)				
	CS DL(L)	chip select for DLART				MEM CD<1:0>H	indicates a write to memory				
	CS MAP(L)	chip select for MAP				MEMWR(L)					

[illegible]

B REV	NUMBER 5416744-0-0	DD CODE	B SIZE
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[illegible]

TV



W1W2 ARE NOT INSTALLED.
2. H2 AND J4 ARE MOUNTED ON SIDE 2
3. MOUNT I13 TO ITEM 16 WITH ITEM 15 BEFORE
SOLDERING YTO ITEM 1
3. TEST PANEL IN TESTER AFTER COMPLETING NOTE 3
AND BEFORE ASSEMBLY OF ITEMS 11, 15, 21, 6 WITH ITEM 17.

STEP	E	X	Y	AXIS	STEP	T	THMS
1	REPEAT	→	X	AXIS	STEP	T	THMS

CHY	CHANCE NO	REV
100	SAIG/AA/1W	B
100	DEFRY 24-MAR-85	
	M.DEMARE	

ETCH REV. AI

[illegible]

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION		REFERENCE DESIGNATOR
						01	A1	
1	1	D-MD-5016743-0-0	5016743-01		CIRCUIT DRILL AND ETCH	1		
2	2		1216565-02		SKT,IC 14PIN DIP TIN ELEV	1		XE1
3	3		1217727-00		PCB,HEADER 20POS(1X20).100CC STR	1		J2
4	4		1219245-01		BATTERY,3CELL 3.75V .18MA NICAD	1		
5	5		1219251-00		PCB HEADER 02PIN(1X02).100CC STR	1		J1
6	6		1219573-05		CONN,D SUB 9PIN ASSY STR	1		J4
7	7		1219952-08		PCB HEADER 09PIN(2X05).100CC STR	1		J3
8	8		1223262-01		SW,ROT 1P08POS	1		S1
9	9		1223263-02		SW,ROT 2P03POS	1		S2
10	10		1223646-01		SW,RKR SPDT ON-OFF-ON	1		S3
11	11		1300229-00		100.0 .25 W 5.0 % CF	1		R1
12	12		1300354-00		750.0 .50 W 5.0 % CF	1		R2
13	13		1912803-00		LS04 INVERTER GATE,HEX	1		E2
14	14		1916921-00		HEXADECIMAL DISPLAY W/DECODER	1		E1
15	15		7430801-01		HOLDER,BATTERY	1		
16	16		7431737-01		PLATE,CONNECTOR	1		
17	17		9008181-01		SCREW,TAP PAN PHIL 6-	4		
18	18		9008451-01		SCREW LOCK,STANDOFF ONLY .060TH	2		

REVISION HISTORY			BASIC PART NO: 5416744			D I G I T A L		
ENG	ECO NUMBER	REV	SECTION A OF A	DRN:	E. LANDRY	DATE:	01-JUN-84	
---	INITIAL	A	SECTION VARIATION INDEX	CHK'D:	D. DROZD	DATE:	01-JUN-84	TITLE PARTS LIST
			[A] 01					FUNCTION SEL/SLU MODULE
			[B]					
			[C]	DES.ENG:	M. DEMARE	DATE:	12-OCT-84	DOCUMENT NUMBER
			[D]					SIZE CODE NUMBER REV
			[E]					
			[F]	RESP.ENG.:	M. DEMARE	DATE:	12-OCT-84	K PL 5416744-0-DBP A
			[H]					
			[J]					
			[K]	MFG.ENG.:	S. WASH	DATE:	12 NOV 84	RELEASE DATE: 27-FEB-85
			[L]					
			[M]	ASSEMBLY NUMBER:		TOP DOCUMENT NUMBER:		FILE NAME: EDIT #
			[N]	D-UA-5416744-0-0		D-UA-5416744-0-0P		ML769A.PLS 34

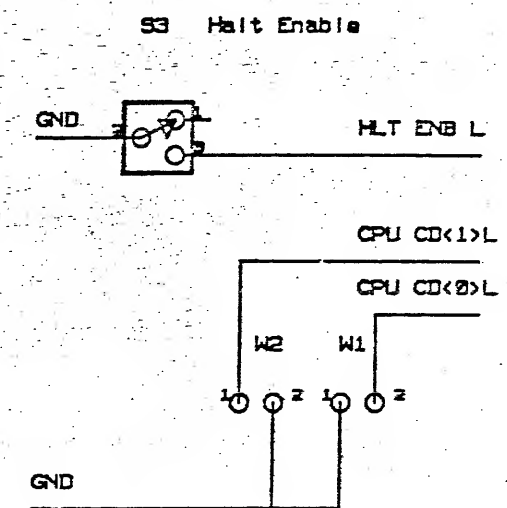
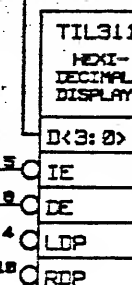
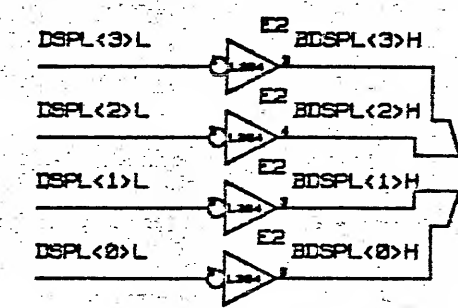
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FROM M7808	TO FS&SLU	FROM M7808	TO FS&SLU
J2 PIN	J2 PIN	J2 PIN	J2 PIN
1	20 GND	11	18 DSPL<3>L
2	19 GND	12	9 GND
3	18 GND	13	8 BDG CD<0>L
4	17 CPU CD<0>L	14	7 BDG CD<1>L
5	16 CPU CD<1>L	15	6 HLT ENB L
6	15 GND	16	5 GND
7	14 DSPL<0>L	17	4 BRS<0>L
8	13 DSPL<1>L	18	3 BRS<1>L
9	12 DSPL<2>L	19	2 BRS<2>L
10	11 BTRYV H	20	1 +5.0V = VCC

FROM M7808	J2	TO FS&SLU
VCC	1	2 BRS<2>L
BRS<1>L	3	4 BRS<0>L
GND	5	6 HLT ENB L
BDG CD<1>L	7	8 BDG CD<0>L
BTRYV H	9	10 DSPL<3>L
DSPL<1>L	11	12 DSPL<2>L
GND	13	14 DSPL<0>L
CPU CD<2>L	15	16 CPU CD<1>L
	17	18
	19	20

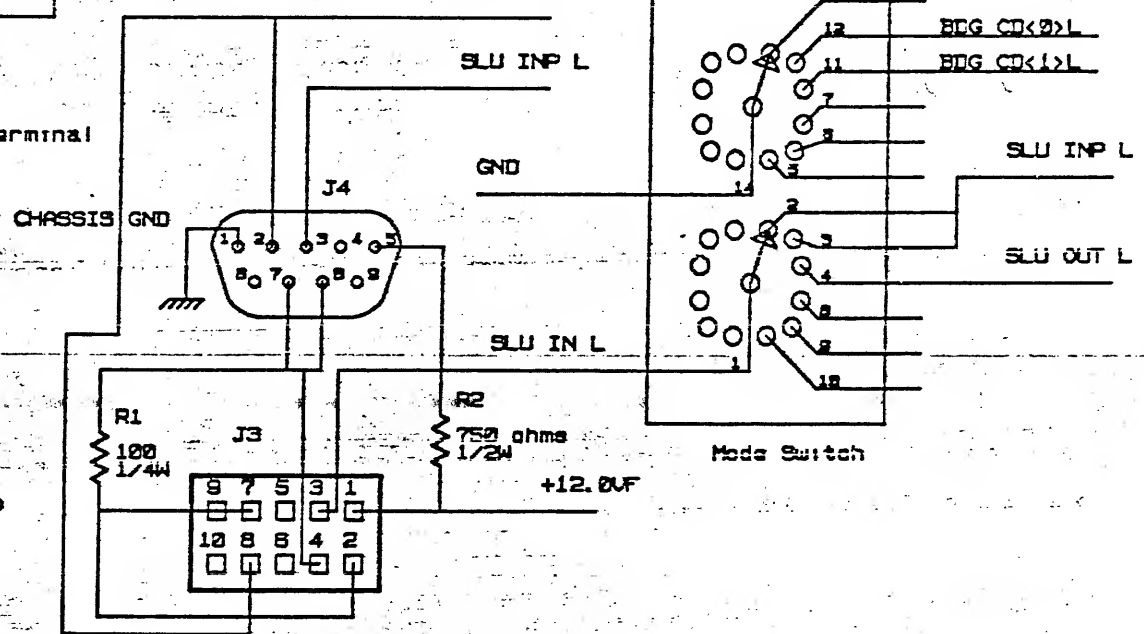
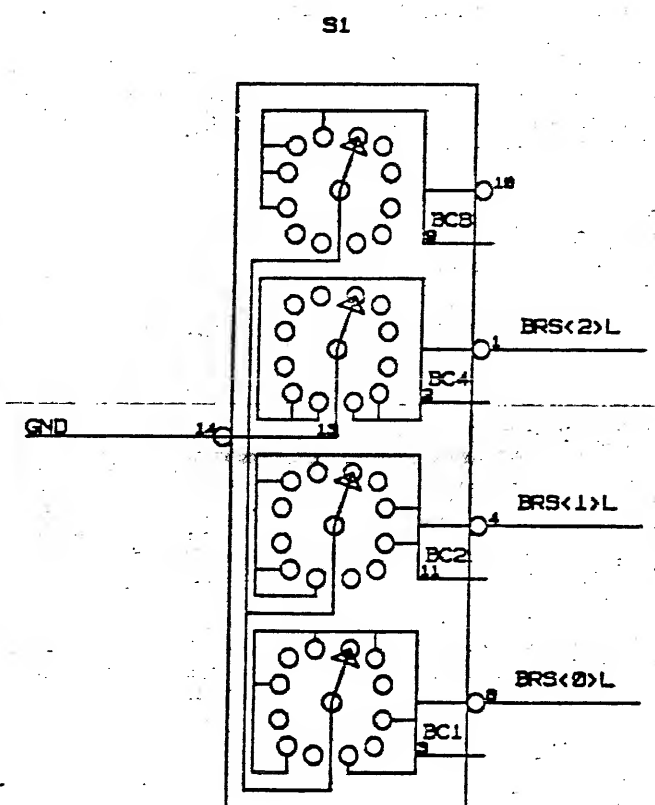
BRS<2>0>L	BDG CD<1:0>L
0 HH 320 BAUD	0 HH NORMAL
1 HL 800	1 HL LANGUAGE INQUIRY
2 HL 1200	2 LH SLU LOOPBACK TEST
3 HL 2400	
4 LH 4800	
5 LH 9600	
6 LH 19200	
7 LL 38400	

FROM M7808	TO FS&SLU
J3 PIN	J3 PIN
1	10 BURESET<L>
2	9 GND
3	8 SLU OUT L
4	7 GND
5	6 KEY
3	5 KEY
7	4 SLU IN H
8	3 SLU IN L
9	2 GND
10	1 +12.0V



W2	W1	FUNCTION
R	R	NORMAL
R	I	AUXILIARY 1
I	R	AUXILIARY 2
I	I	AUXILIARY 3
		I=INSERTED R=REMOVED

BDG CD<1:0>L
0 HH NORMAL
1 HL LANGUAGE INQUIRY
2 LH SLU LOOPBACK TEST



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0 - 0 - 0 - 0 - 0 - 0 - 0 - 0
UA 2

COMPONENT SIDE VIEW

2
(QTY. 4)

5187 REF
129.54 MM.

841 REF
213.36 MM.

NOTES:

STEP E → Y AXIS _____ STEP _____ TIMES
REPEAT → X AXIS _____ STEP _____ TIMES

CHK	CHANGE NO	REV
142	140014M.001	B
142	140014M.001	B
142	140014M.001	B
142	140014M.001	B
142	140014M.001	B
142	140014M.001	B
142	140014M.001	B
142	140014M.001	B
142	140014M.001	B
142	140014M.001	B

ETCH REV.	B1-P2
-----------	-------

SIGNATURES	DATE	TITLE
DRN. E. LANDRY	7-2-85	digital
CHK'D. R. LANDRY	7-2-85	
MECH. ENG. R. LANDRY	5-10-85	
PROJ. ENG. R. LANDRY	5-10-85	
PROD. R. LANDRY	5-10-85	
SCALE 2:1		
SHT. 1 OF 1		
NEXT HIGHER ASSY. B-DD-M9047-0-0		

SIZE	CODE	NUMBER	REV
D	UA	M9047-0-0	B

1 MS# 275466

8 6 5 4 3 2 1

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AM2
AN2
AR2
AS2

REV. A
DCS M9047-0-1

DATE ECO NUMBER REV.

DWG 1026

8 7 6 5 4 3 2 1

digital

GRANT CONTINUITY

DOCUMENT NUMBER

DCS M9047-0-1 A

B-D0-M9047-0-0

AUTOMATED BY		PRTLST.5R(55)		PARTS LIST		QTY PER VARIATION	
LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	01	02
						VARIATION REVISION LEVEL:	
1	1	A-PS-1700313-0-0	1700313-01	A	CABLE ASSY,06 COND,MOLD,SHLD	2	1
2	2	A-PS-4700042-0-0	4700042-01		SCREWDRIVER,FLAT BLADE 0.12 X 2.		1
3	3	A-PS-3622092-0-0	3622092-01	A	LABEL,LCP5 CONFIGURATION		1
4	4	A-PS-9907349-0-0	9907349-01	A	CARTON,DIECUT,C,200PSI,W/GRAPHIC		1
5	5	B-DD-M9047-0	M9047-00		QBUS GRANT CONTINUITY,1ST USED I		1
6	6	A-PS-1700301-0-0	1700301-00	A	CABLE ASSY,07 COND,MOLD,SHLD	2	1
7	7	A-PS-3624251-0-0	3624251-01	A	LABEL,FRONT CONTROL PANEL BA123		1

REVISION HISTORY			BASIC PART NO: 7022382		DRN: D. HEALY	DATE: 05-DEC-84	D I G I T A L	
ENG	ECO NUMBER	REV	SECTION A OF A		CHK'D: D. HEALY	DATE: 08-MAR-85	TITLE PARTS LIST BA123-A ACCESSORY KIT	
---	INITIAL	A	SECTION VARIATION INDEX (A)01,02		DES.ENG: J. KWONG	DATE: 08-MAR-85	DOCUMENT NUMBER	
			(B)		RESP.ENG.: J. KWONG	DATE: 08-MAR-85	SIZE	CODE
			(C)		MFG.ENG.: J. EDWARDS	DATE: 08-MAR-85	K	PL
			(D)		ASSEMBLY NUMBER:	TOP DOCUMENT NUMBER:	7022382-0-DBP	
			(E)				RELEASE DATE: 26-MAR-85	
			(F)				FILE NAME:	EDIT #
							ML755A.PLS	4
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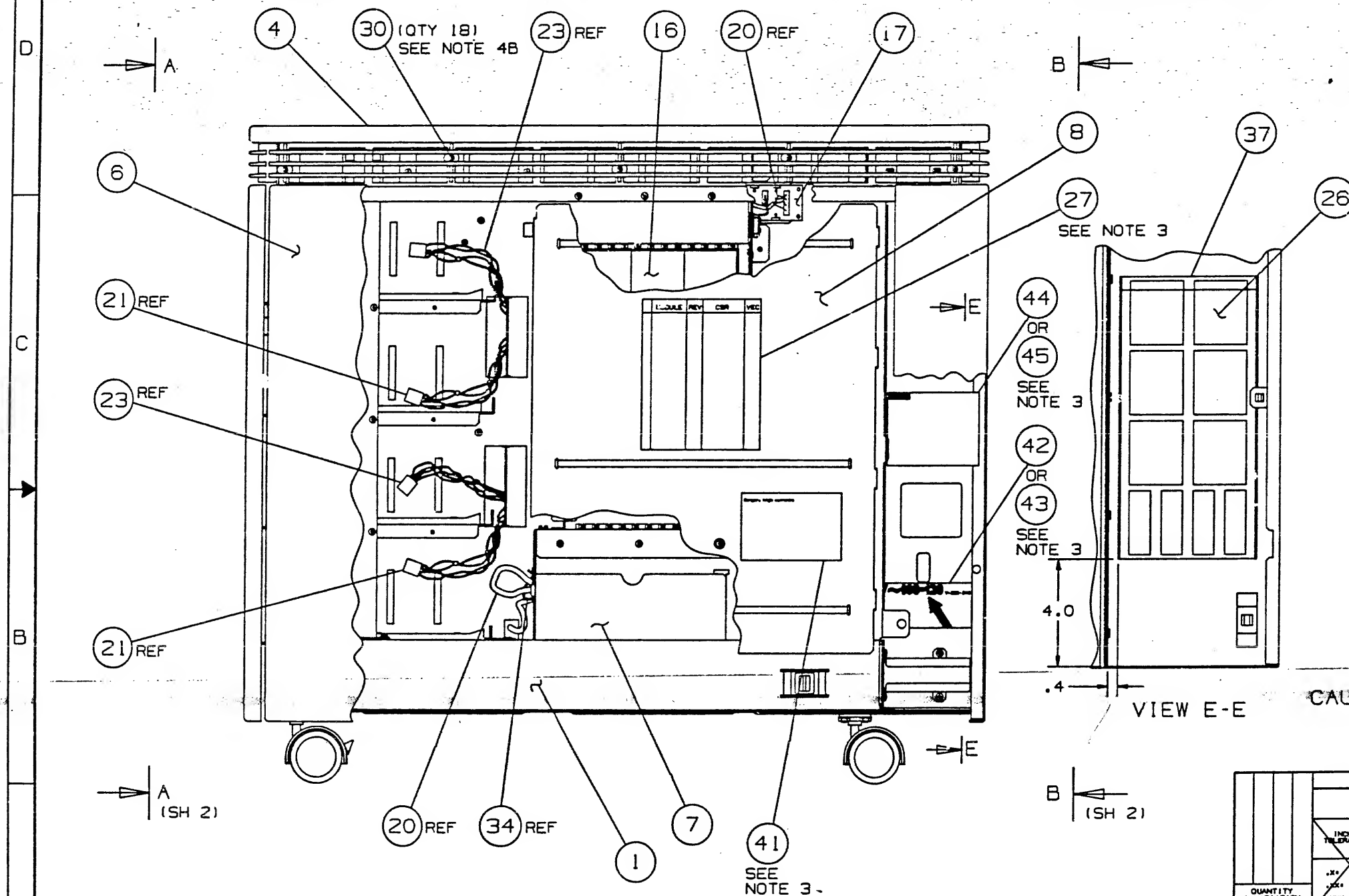
MLO 1

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LEGEND		
PART NO.	REV	V. RATION
7022380-01	A1	120V
7022380-02	A1	240V

NOTES:

1. ITEM #12 (LOUVRE, SHORT) TO BE ORIENTATED BY ITS MARKING LOCATED ON THAT ITEM.
2. ITEMS #34 (CABLE CLAMP) TO BE LOCATED APPROX WHERE SHOWN.
3. LOCATE ITEMS 27, 41, 42 OR 43, 44 OR 45 APPROX WHERE SHOWN NEAR SIDE.
4. TORQUE REQUIREMENTS ARE AS FOLLOWS:
 - A. ITEMS #31, 32 & 36 SHALL BE 8 TO 11 INCH-LBS
 - B. ITEM #30 TO BE 6 TO 8 INCH-LBS
 - C. ITEM #29 TO BE 18 TO 24 INCH-LBS.
5. WORKMANSHIP TO BE PER DEC STD 187

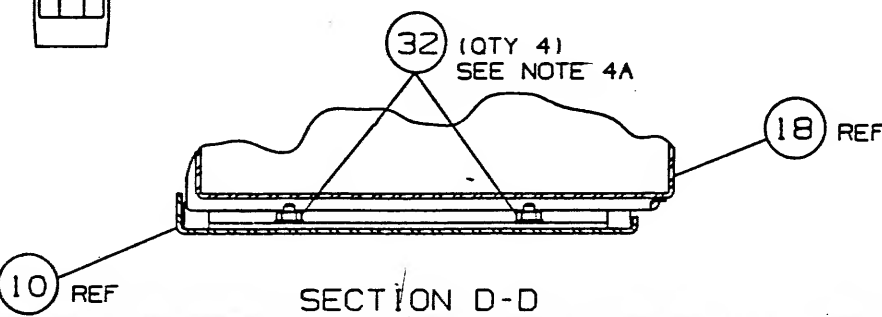
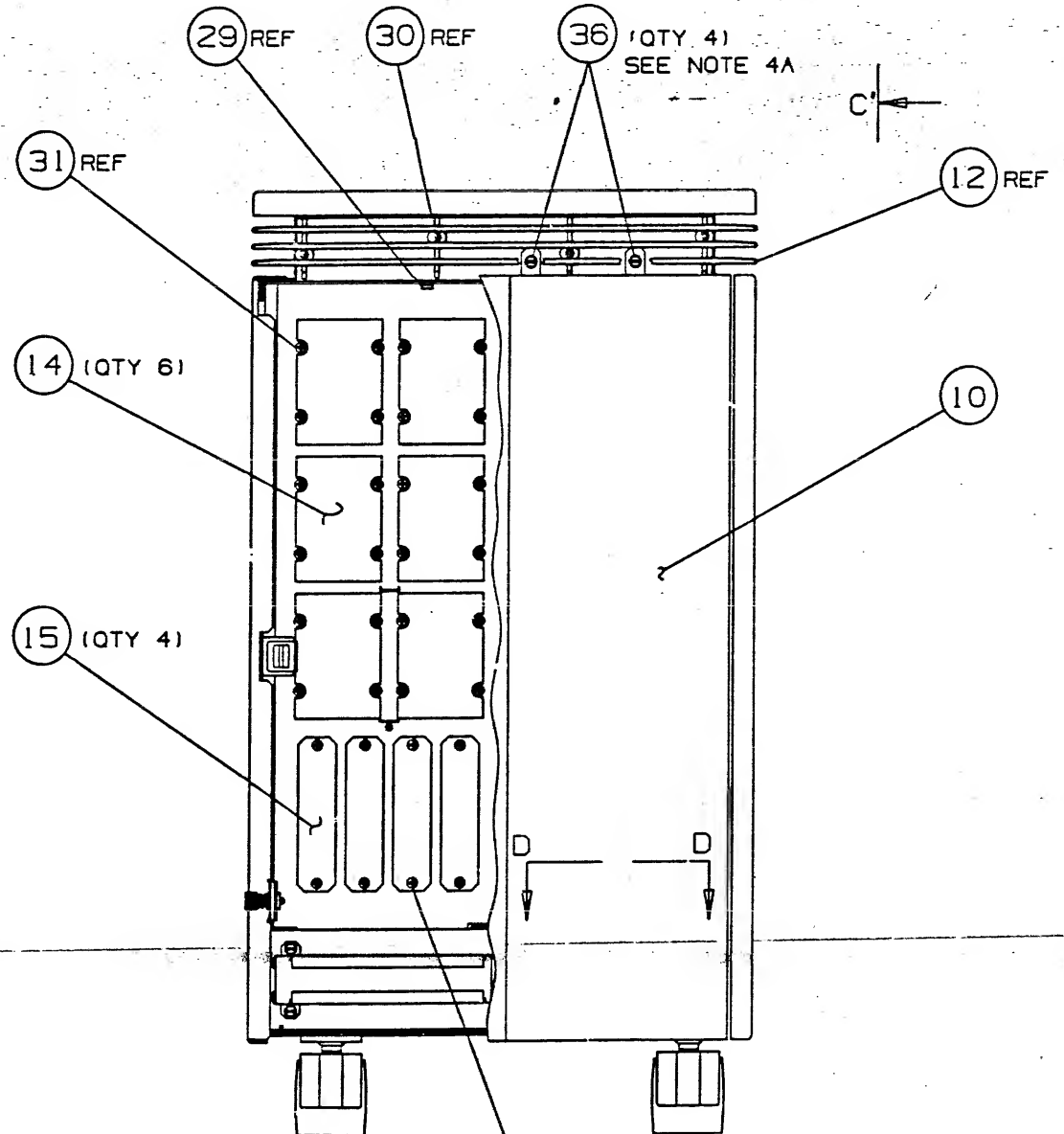
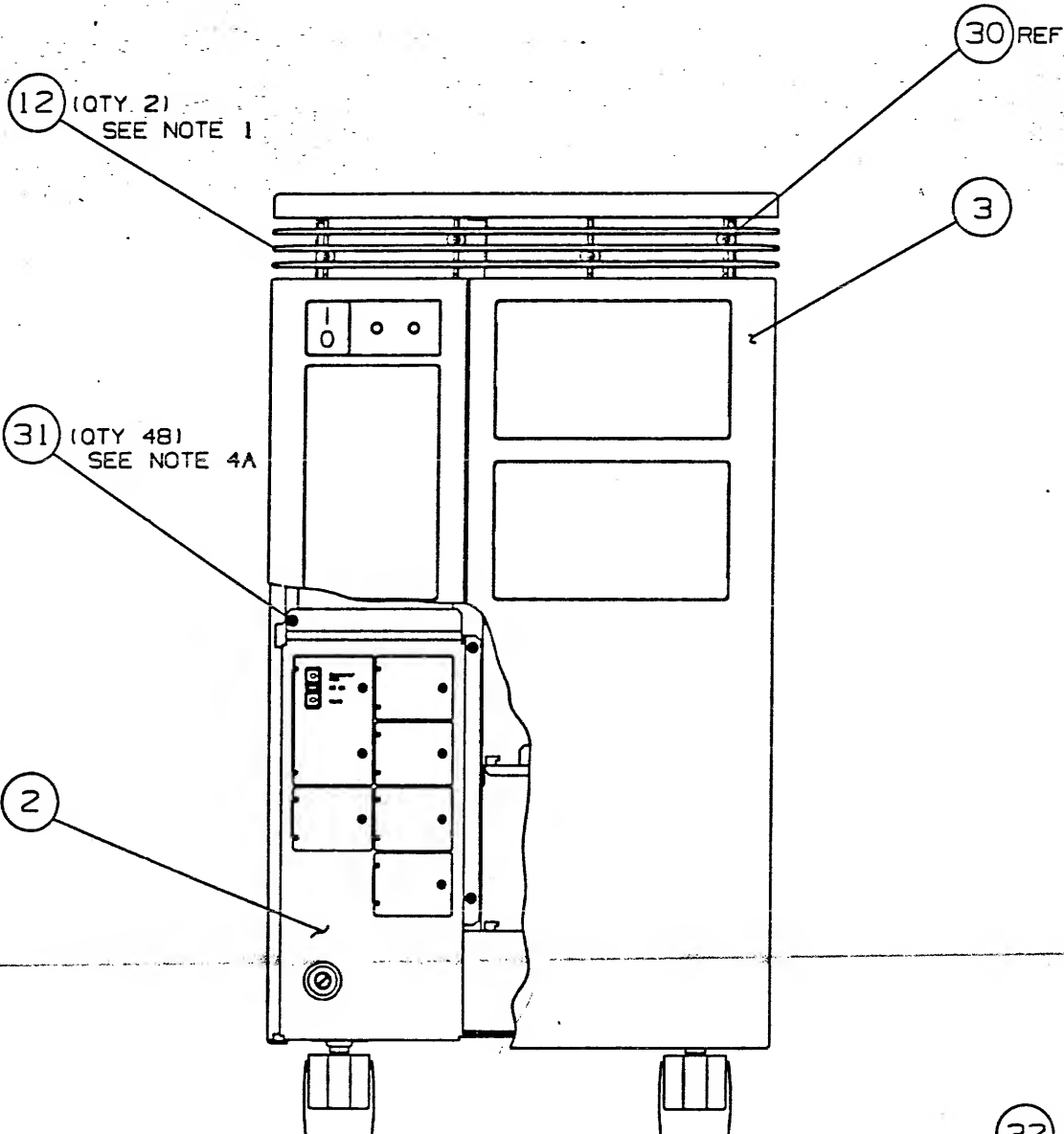


CAUTION: OFF SHEET PARTS LIST EXISTS
REFER TO K-PL-7022380-0-DBP
(ML 752)

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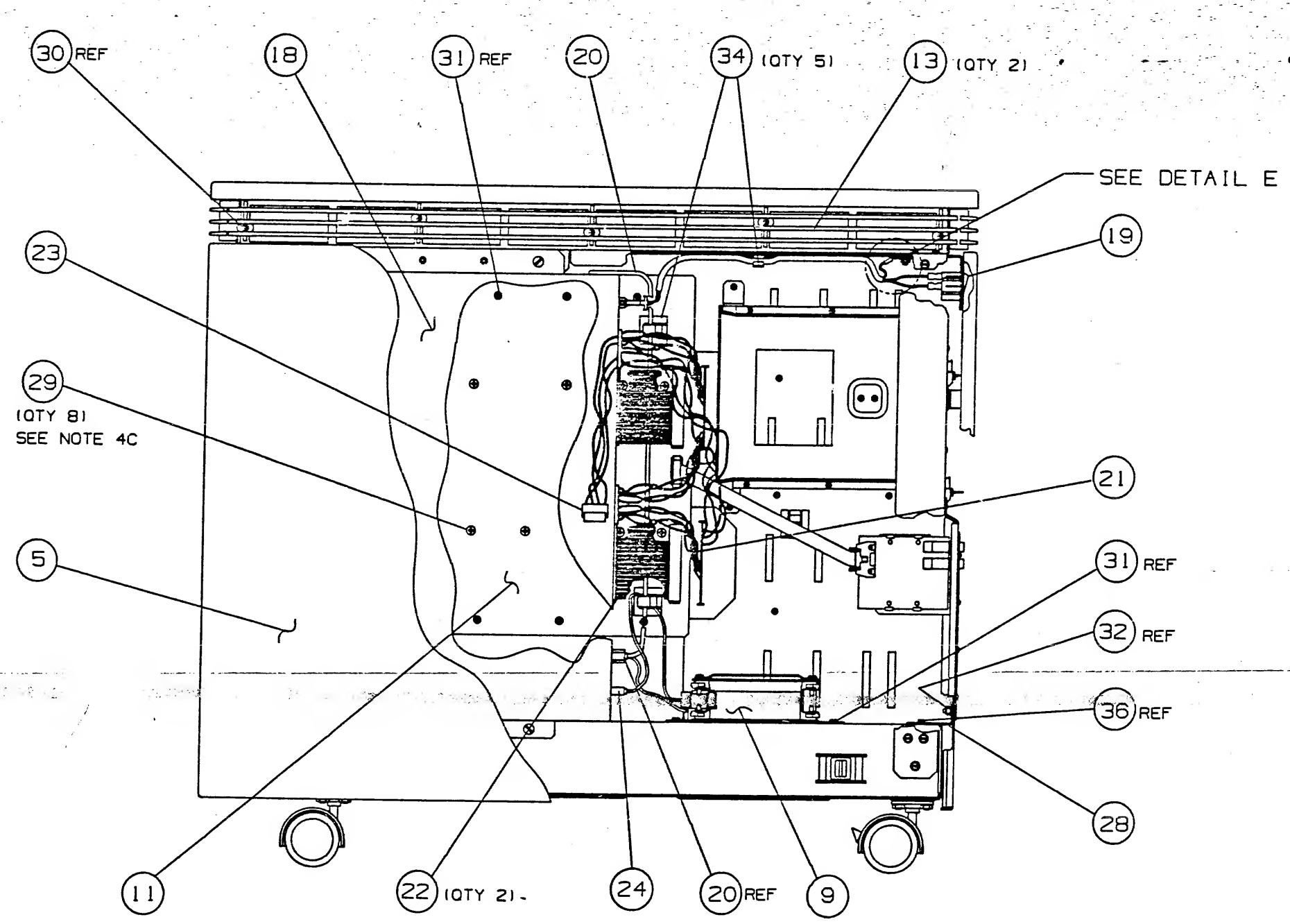


REVISIONS		
CHK	CHANGE NO	REV
	RELEASE	B

TITLE		SIZE/CODE	NUMBER	REV
BA123-A BASIC ENCLOSURE		D AD	7022380-0-DBU	B
SCALE	1/2	SHEET	2 OF 3	DIST

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7022380-0-DBU
DIV 2



DETAIL E
SCALE 1/1

VIEW C-C

REVISIONS		
CHK	CHANGE NO	REV
	RELEASE	B

TITLE		BA123-A BASIC ENCLOSURE	SIZE CODE	D AD	NUMBER	7022380-0-DBU	REV	B
SCALE	1/2	SHEET	3	OF	3	DIST		

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION	
						01	02
						VARIATION REVISION LEVEL:	
						A1	A1
1	1	D-AD-7021991-0-DBU	7021991-01		FRAME ASSEMBLY	1	1
2	2	C-AD-7021996-0-DBU	7021996-01		CONTROL PANEL ASSY.	1	1
3	3	D-AD-7021997-0-DBU	7021997-01		PANEL COVER FRONT DISK ASSY	1	1
4	4	D-AD-7021999-0-DBU	7021999-01		TOP COVER ASSY.	1	1
5	5	D-AD-7022000-0-DBU	7022000-01		SIDE PANEL ASSY L/H	1	1
6	6	D-AD-7022001-0-DBU	7022001-01		SIDE PANEL ASSY R/H	1	1
7	7	D-AD-7022003-0-DBU	7022003-01		FAN MOUNT CARD CAGE ASSY.	1	1
8	8	D-IA-7022006-0-DBU	7022006-01		COVER FRONT CARD CAGE ASSY.	1	1
9	9	D-AD-7022296-0-DBU	7022296-01		FAN MOUNT MASS STORAGE ASSY	1	1
10	10	D-AD-7022339-0-DBU	7022339-01		DOOR, REAR ASSY.	1	1
11	11	D-IA-7430692-0-DBU	7430692-01		COVER,REAR,CARD CAGE	1	1
12	12	D-MD-7430709-0-DBU	7430709-01		LOUVRE,SHORT	2	2
13	13	D-MD-7430710-0-DBU	7430710-01		LOUVRE, LONG	2	2
14	14	C-IA-7427574-0-0	7427574-01		PLATE,COVER	6	6
15	15	B-MD-7428683-0-DBU	7428683-01		PLATE,CONNECTOR BLANK	4	4
16	16	E-UA-5417507-0-DBU	5417507-01		QBUS BACKPLANE,13 SLOTS,QUAD	1	1
17	17	D-UA-5416665-0-DBU	5416665-01		REMOTE SENSE OF TEMPERATURE FOR	1	1
18	18	D-PS-3023616-0-DBU	3023616-01		P.S. 460W 2DC REGULATOR BDS,FAN	1	1
19	19	A-PS-1700859-0-0	1700859-01		CABLE ASSY,AC,ON/OFF POWER	1	1
20	20	A-PS-1700863-0-0	1700863-01		CABLE ASSY,FAN	1	1
21	21	A-PS-1700870-0-0	1700870-01		CABLE ASSY,DC POWER DRIVE	1	1
22	22	A-PS-1700865-0-0	1700865-01		CABLE ASSY,18COND	2	2
23	23	A-PS-1700911-0-0	1700911-01		CABLE ASSY,9POS POWER DRIVE	1	1
24	24	A-PS-1700864-0-0	1700864-01		CABLE ASSY,FAN	1	1
25	25	A-PA-3700821-0-0	3700821-01		PKG COMPUTER, BA123 CUSTOMER	1	1
26	26	A-PS-3624253-0-0	3624253-01		LABEL,I/O,BULKHEAD	1	1
27	27	A-PS-3624254-0-0	3624254-01		LABEL,MU BUSINESS COMPUTER	1	1
28	28	C-MD-7431225-0-DBU	7431225-01		BRACKET,CONTROL PANEL	1	1
29	29		9010174-01		SCREW,SEMS PAN PHIL	8	8
30	30		9000055-01		SCREW,THD RL,PAN POZI F/METL	4	18

REVISION HISTORY		BASIC PART NO: 7022380		DRN: S. STEFANICK		DATE: 18-DEC-84		D I G I T A L	
ENG	ECO NUMBER	REV	SECTION A OF A	CHK'D: J. KUSHAGIN		DATE: 13-FEB-85		TITLE PARTS LIST	
	INITIAL	B	SECTION VARIATION INDEX					BA123-A BASIC ENCLOSURE	
			[A]01,02						
			[B]	DES.ENG: J. KWONG		DATE: 18-DEC-84		DOCUMENT NUMBER	
			[C]					SIZE CODE NUMBER REV	
			[D]	RESP.ENG.: J.KWONG		DATE: 18-DEC-84		K PL 7022380-0-DBP B	
			[E]	MFG.ENG.: J. EDWARDS		DATE: 18-DEC-84		RELEASE DATE: 06-MAR-85	
			[F]	ASSEMBLY NUMBER:		TOP DOCUMENT NUMBER:		FILE NAME: EDIT #	
				B-DD-7022380-0-DBU		B-DD-7022380-0-DBU		ML752B.PLS 23	

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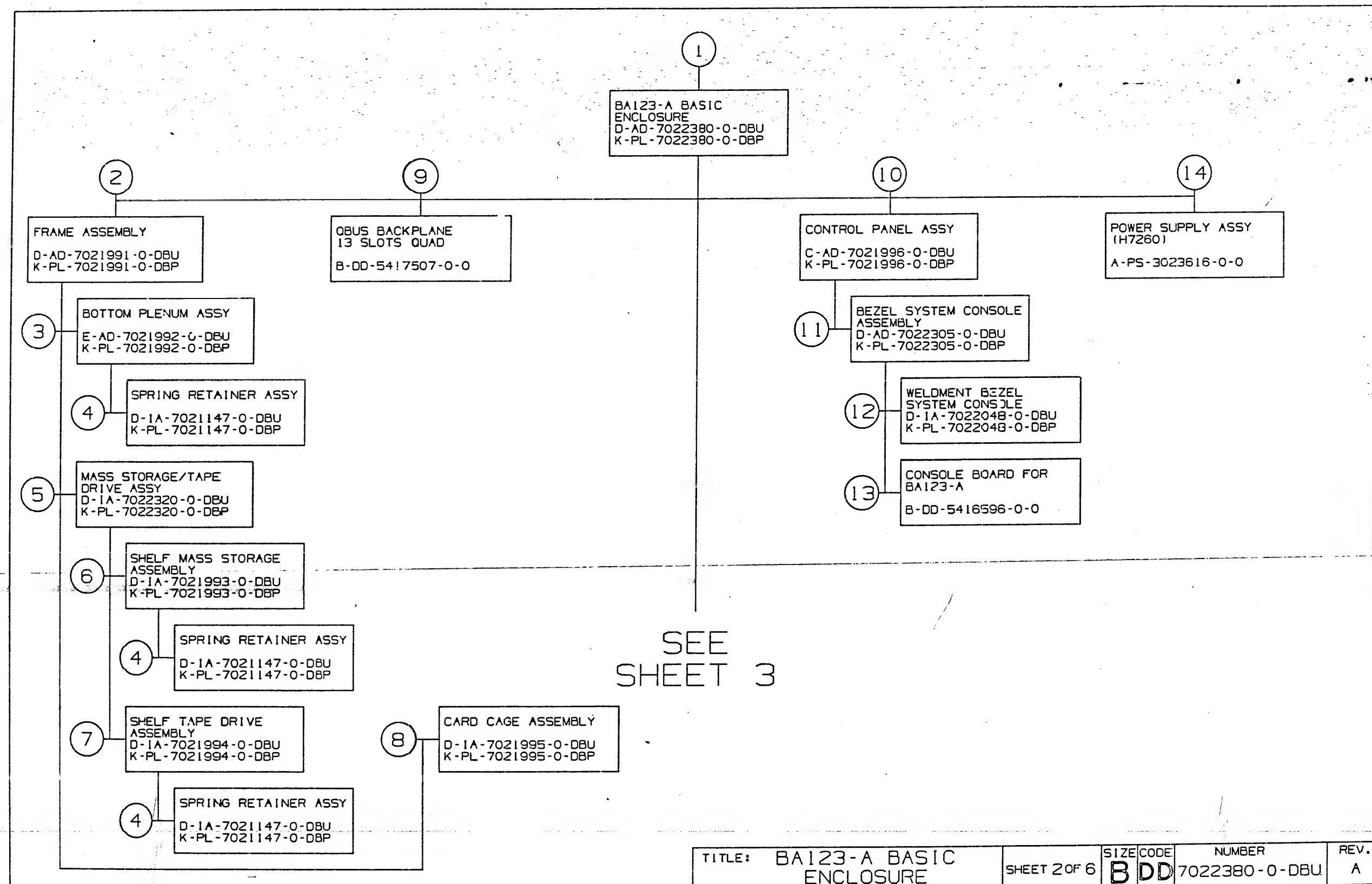
LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION	
						01	02
					VARIATION REVISION LEVEL:	A1	A1
31	31		9009701-00		SCREW,SEMS PAN PHIL-- 6-	48	48
32	32		9006560-00		NUT,HEX EXT TOOTH LCKWSHR 6-32	4	4
33	33		9007651-00		WASHER,LOCK EXTERNAL STEEL	1	1
34	34		9010016-00		CLAMP, CABLE, ADH BACK	5	5
35	35		9006565-00		NUT,HEX EXT TOOTH LCKWSHR 10-32	1	1
36	36		9010075-03		SCREW,TAP HEXWW THD RL 6-	4	4
37	37		9907588-01		ENVELOPE,CLEAR ADH BACK	1	1
38	38	D-AR-7022380-0-DBU			BA123-A SYSTEM ARRANGEMENT	REF	REF
39	39	K-SP-BA123-A-DBF			ENG. SPEC BA123-A	REF	REF
40	40		1700083-00		PWR CORD,TERM 3-14 SJT 125	1	-
41	41		3615087-04		LABEL,"DANGER-HIGH CURRENT"	1	1
42	42		3617905-16		LABEL,WARNING EQUIP. RATING,100-	1	-
43	43		3617905-17		LABEL,WARNING EQUIP. RATING,220-	-	1
44	44	A-PS-3624471-0-0	3624471-01		LABEL,BUSINESS COMP BA123-A2	1	-
45	45	A-PS-3624471-0-0	3624471-02		LABEL,BUSINESS COMP BA123-A3	-	1

46 NOTE: ITEMS #25 AND #40 NOT SHOWN ON FIELD OF DWG.

D I G I T A L	TITLE	BA123-A BASIC ENCLOSURE	SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
				K	PL	7022380-0-DBP	B

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ML01



TITLE: BAI23-A BASIC ENCLOSURE

SHEET 2 OF 6

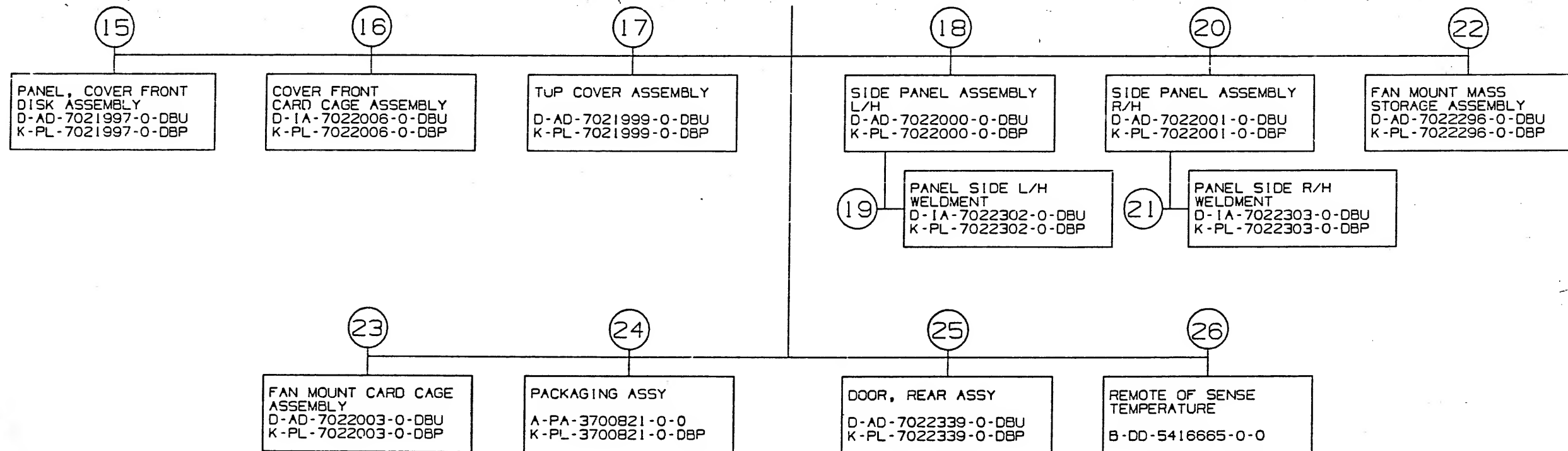
SIZE CODE
B DD

NUMBER
7022380-0-DBU

REV.
A

MLO 1

CONT FROM SHEET 2



TITLE: BA123-A BASIC
ENCLOSURE

SHEET 3 OF 6

SIZE CODE
B DD

NUMBER
7022380-0-DBU

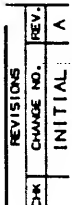
REV.
A

MLO1

FIND NO.	DRAWING NO.	DESCRIPTION	TYPE	FIND NO.	DRAWING NO.	DESCRIPTION	TYPE
					A-SS-7022048-0-1	SILK SCREEN	M
7	D-1A-7021994-0-DBU	SHELF TAPE DRIVE ASSEMBLY	M	13	B-DD-5416596-0-0	CONSOLE BOARD FOR BAI23-A	E/M
	K-PL-7021994-0-DBP	SHELF TAPE DRIVE ASSEMBLY (PL)	M				
	D-MD-7430746-0-DBU	SHELF TAPE DRIVE	M				
	D-MD-7427554-0-DBU	HALF SLIDE	M				
				14	A-PS-3023616-0-0	POWER SUPPLY ASSEMBLY (H7260)	E/M
8	D-1A-7021995-0-DBU	CARD CAGE ASSEMBLY	M				
	K-PL-7021995-0-DBP	CARD CAGE ASSEMBLY (PL)	M				
	E-1A-7430690-0-DBU	FRAME CARD CAGE	M	15	D-AD-7021997-0-DBU	PANEL COVER FRONT DISK ASSY	M
	K-PL-7430690-0-DBP	FRAME CARD CAGE (PL)	M		K-PL-7021997-0-DBP	PANEL COVER FRONT DISK ASSY (PL)	M
	D-MD-7429632-0-DBU	CARD GUIDE 12 SLOT	M		E-MD-7430704-0-DBU	PANEL, FRONT	M
	D-1A-7430693-0-DBU	BAFFLE, FCC	M		C-MD-7431191-0-DBU	BRACKET, STUD	M
	K-PL-7430693-0-DBP	BAFFLE, FCC (PL)	M		E-MD-7430708-0-DBU	DOOR, FRONT	M
					C-MD-7431178-0-DBU	BRACKET, DOOR HINGE	M
					D-MD-7431477-0-DBU	PANEL, FILLER	M
9	B-DD-5417507-0-0	OBUS BACKPLANE 13 SLOTS QUAD	E/M				
10	C-AD-7021996-0-DBU	CONTROL PANEL ASSEMBLY	M	16	D-1A-7022006-0-DBU	CARD CAGE FRONT COVER ASSY	M
	K-PL-7021996-0-DBP	CONTROL PANEL ASSEMBLY (PL)	M		K-PL-7022006-0-DBP	CARD CAGE FRONT COVER ASSY (PL)	M
	E-1A-7430705-0-DBU	PANEL CONTROL	M		E-1A-7430691-0-DBU	COVER FRONT CARD CAGE	M
	K-PL-7420705-0-DBP	PANEL CONTROL (PL)	M		K-PL-7430691-0-DBP	COVER FRONT CARD CAGE (PL)	M
	C-MD-7431171-0-DBU	BEZEL, BLANK	M		D-MD-7430828-0-DBU	SUPPORT MODULES	M
					D-MD-7431479-0-DBU	SUPPORT, MODULE REMOVEABLE	M
11	D-AD-7022305-0-DBU	BEZEL, SYSTEM CONSOLE ASSY	E/M	17	D-AD-7021999-0-DBU	TOP COVER ASSEMBLY	M
	K-PL-7022305-0-DBP	BEZEL, SYSTEM CONSOLE ASSY (PL)	E/M		K-PL-7021999-0-DBP	TOP COVER ASSEMBLY (PL)	M
	A-PS-1700860-0-0	CABLE ASSY, CONSOLE BACKPLANE	E/M		D-1A-7430707-0-DBU	COVER, TOP	M
					K-PL-7420707-0-DBP	COVER, TOP (PL)	M
					C-MD-7423357-0-DBU	KEY BUTTON	M
					D-1A-7431045-0-DBU	BRACKET, COVER	M
					K-PL-7431045-0-DBP	BRACKET, COVER (PL)	M
12	D-1A-7022048-0-DBU	WELDMENT, BEZEL SYS CONSOLE	M				
	K-PL-7022048-0-DBP	WELDMENT, BEZEL SYS CONSOLE (PL)	M				
	D-MD-7431169-0-DBU	BRACKET, SUPPORT SYSTEM CONSOLE	M				
	D-MD-7431173-0-DBU	BEZEL, SYSTEM CONSOLE	M				
TYPE: E ELECTRICAL M MECHANICAL E/M ELECTRO/MECHANICAL				TITLE: BAI23-A BASIC ENCLOSURE			
				SHEET 5 OF 6			
				SIZE CODE BDD			
				NUMBER 7022380-0-DBU			
				REV. A			

2	D	AR	7022380-0-DBU	A
---	---	----	---------------	---

1. RDX SIGNAL DISTRIBUTION (M9058) IS SHOWN FOR REF ONLY AND NOT PART OF BA123-A. (SEE SHEET 5)
2. FOR REAR PANEL RULES AND CONFIGURATION SEE SHEET 3.
3. FOR POWER HARNESS WIRING DIAGRAM SEE SHEET 6.
4. FOR MODULE RULES SEE SHEET 6.
5. MASS STORAGE CONFIGURATION RULES:
THE POWER SUPPLY IN THE BA123-A ENCLOSURE CAN POWER UP TO FOUR OF THE FIVE DRIVE SLOTS ONLY.
THE FOLLOWING ARE SOME OF THE COMBINATIONS:
 - (4) RD52'S
 - RX50, TK50, (2) RD52'S
 - TK50, (3) RD52'S



PLOT AT .5000

[illegible]

digital

BA123-A
SYSTEM
ARRANGEMENT

DOCUMENT NUMBER			
SIZE	CODE	NUMBER	
D	AR	7022380-0-DBU	
SCALE	1/2	SHEET	OF

MLOI

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DAR 7022380-0-DBU

DAR 7022380-0-DBU

RDXX #4/TK50

RDXX #3

RDXX #2

RDXX #1

→ A
(SEE SHEET 1)

→ A
(SEE SHEET 3)

VIEW C-C
(SEE SHEET 1)
SHOWN WITHOUT FRONT
OR REAR PANELS

REVISIONS		
CHK	CHANGE NO	REV

TITLE BA123-A
SYSTEM ARRANGEMENT

PLOT AT .5000

SIZE CODE D AR NUMBER 7022380-0-DBU REV A

SCALE 1/2

SHEET 2 OF 6

DIST

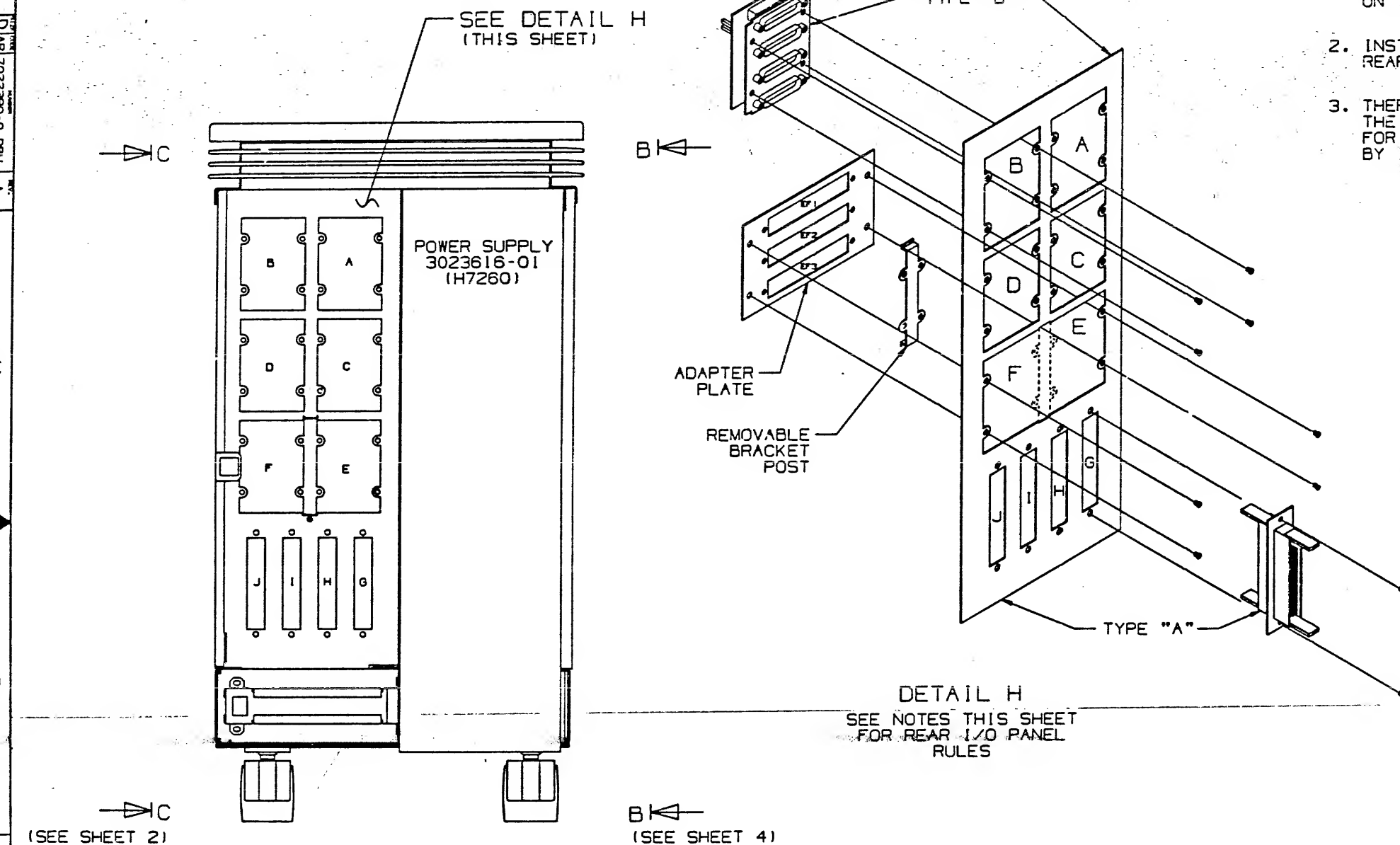
1. MLO1

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NOTES:

REAR I/O PANEL CONNECTION RULES:

1. INSTALL TYPE "B" (2.5" X 3.2") FILTER PANEL ON TO THE REAR I/O PANEL IN THIS SEQUENCE:
A → C → E → B → D → F
2. INSTALL TYPE "A" (1" X 4") FILTER PANEL ON TO REAR I/O PANEL IN THIS SEQUENCE:
G → H → I → J
3. THERE IS A REMOVABLE BRACKET POST BETWEEN THE BOTTOM 2 TYPE "B" CUTOUTS. THIS ALLOWS FOR THE ADDITION OF 3 MORE TYPE "A" CUTOUTS BY INSTALLING AN ADAPTER PLATE (7427720-01)



DETAIL H
SEE NOTES THIS SHEET
FOR REAR I/O PANEL
RULES

VIEW D-D
(SEE SHEET 2)
SHOWN WITHOUT REAR
OR SIDE PANELS

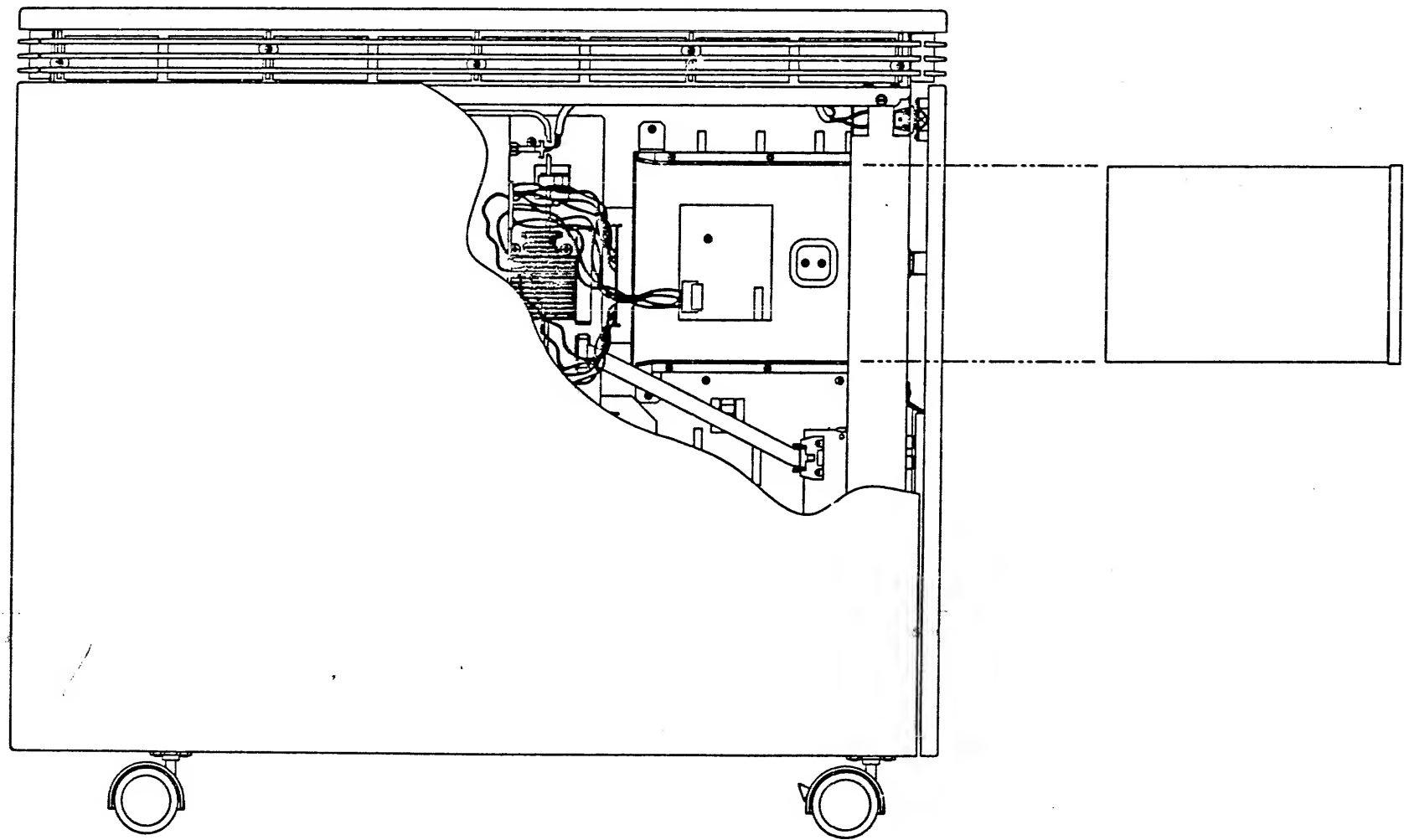
REVISIONS		
CHK	CHANGE NO	REV

PLOT AT .5000

TITLE BAI23-A SYSTEM ARRANGEMENT		SIZE CODE D	NUMBER AR 7022380-0-DBU	REV A
SCALE 1/2	SHEET 3	OF 8	DIST	

MLC1

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VIEW B-B
(SEE SHEET 1)
(TK50 INSTALLATION)

REVISIONS		
CHK	CHANGE NO	REV

TITLE		SIZE/CODE	NUMBER	REV
BA123-A		D	7022380-0-DBU	A
SYSTEM ARRANGEMENT				
SCALE	1/2	SHEET	4	OF 6
DIST				

PLOT AT .5000

MLO1

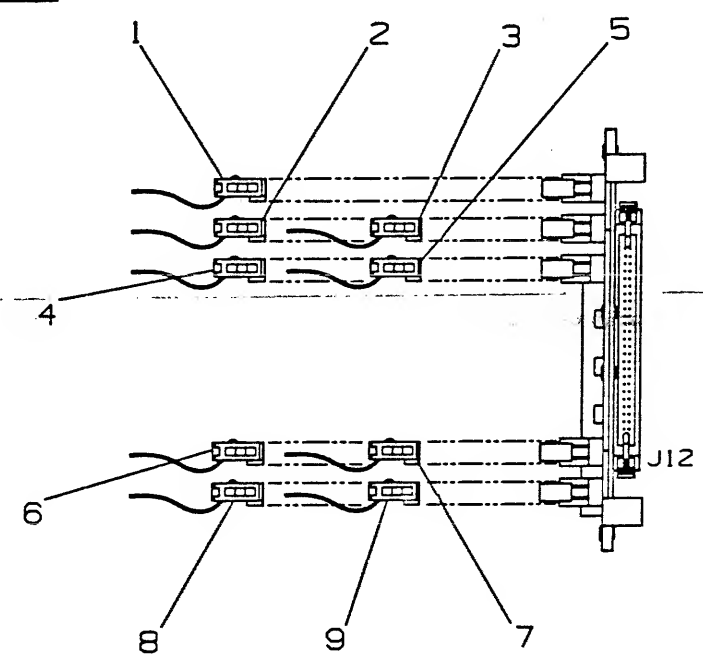
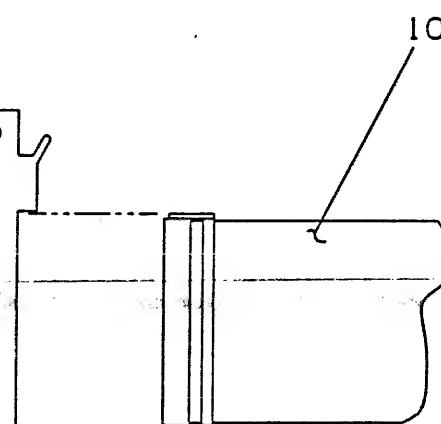
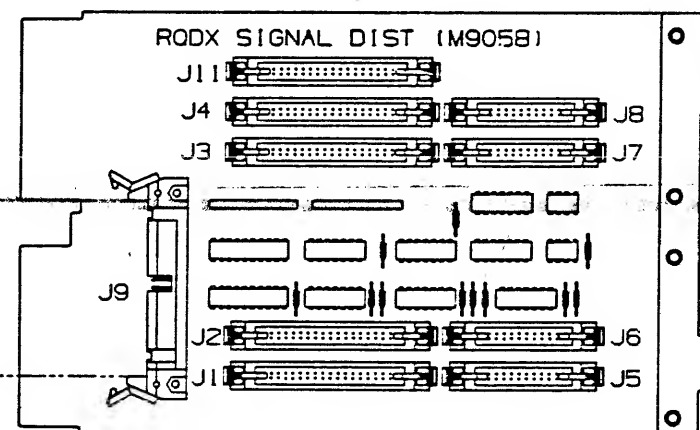
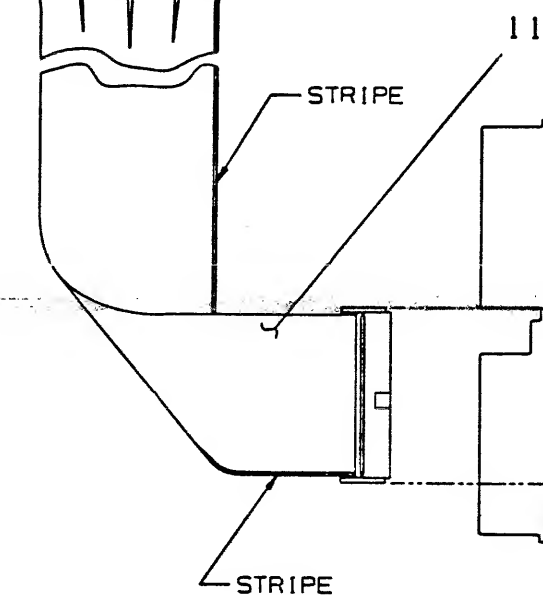
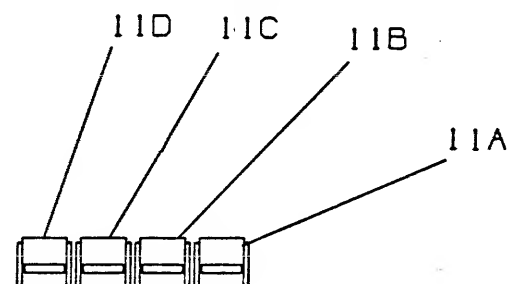
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CABLE LEGEND

ITEM	PART NO.	FROM	TO
1	1700867-01	M9058-J11	RX50
2	1700286-01	M9058-J4	RDXX#4
3	1700282-01	M9058-J8	RDXX#4
4	1700286-01	M9058-J3	RDXX#3
5	1700282-01	M9058-J7	RDXX#3
6	1700286-01	M9058-J2	RDXX#2
7	1700282-01	M9058-J6	RDXX#2
8	1700286-01	M9058-J1	RDXX#1
9	1700282-01	M9058-J5	RDXX#1
10	1700861-01	M9058-J12	RDX2 MODULE
11	1700862-01	M9058-J9	SEE BELOW
11A			RDXX#1 CONSOLE
11B			RDXX#2 CONSOLE
11C			RDXX#3 CONSOLE
11D	1700862-01	M9058-J9	RDXX#4 CONSOLE

NOTES:

1. ITEM #S SHOWN ARE FOR REF ONLY (FOR CABLE HOOK UP ONLY).



REVISIONS		
CHK	CHANGE NO	REV

PLOT AT 1.000

TITLE	BA123-A	SIZE/CODE	NUMBER	REV
	SYSTEM ARRANGEMENT	D AR	7022380-0-DBU	A
SCALE	1/1	SHEET	5 OF 6	DIST

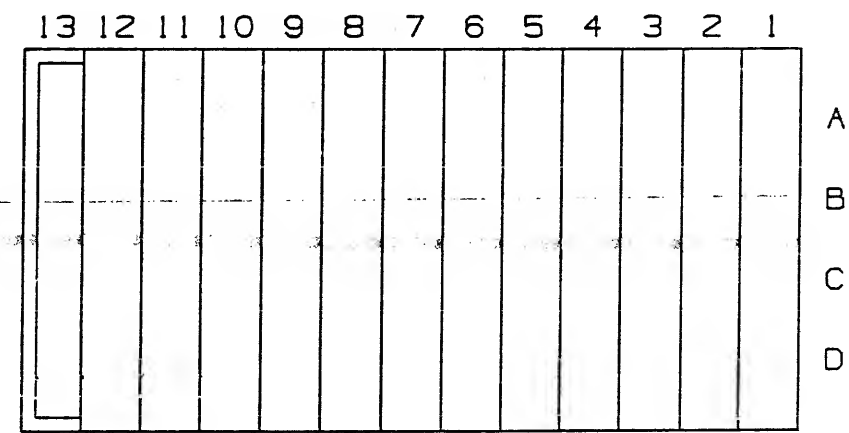
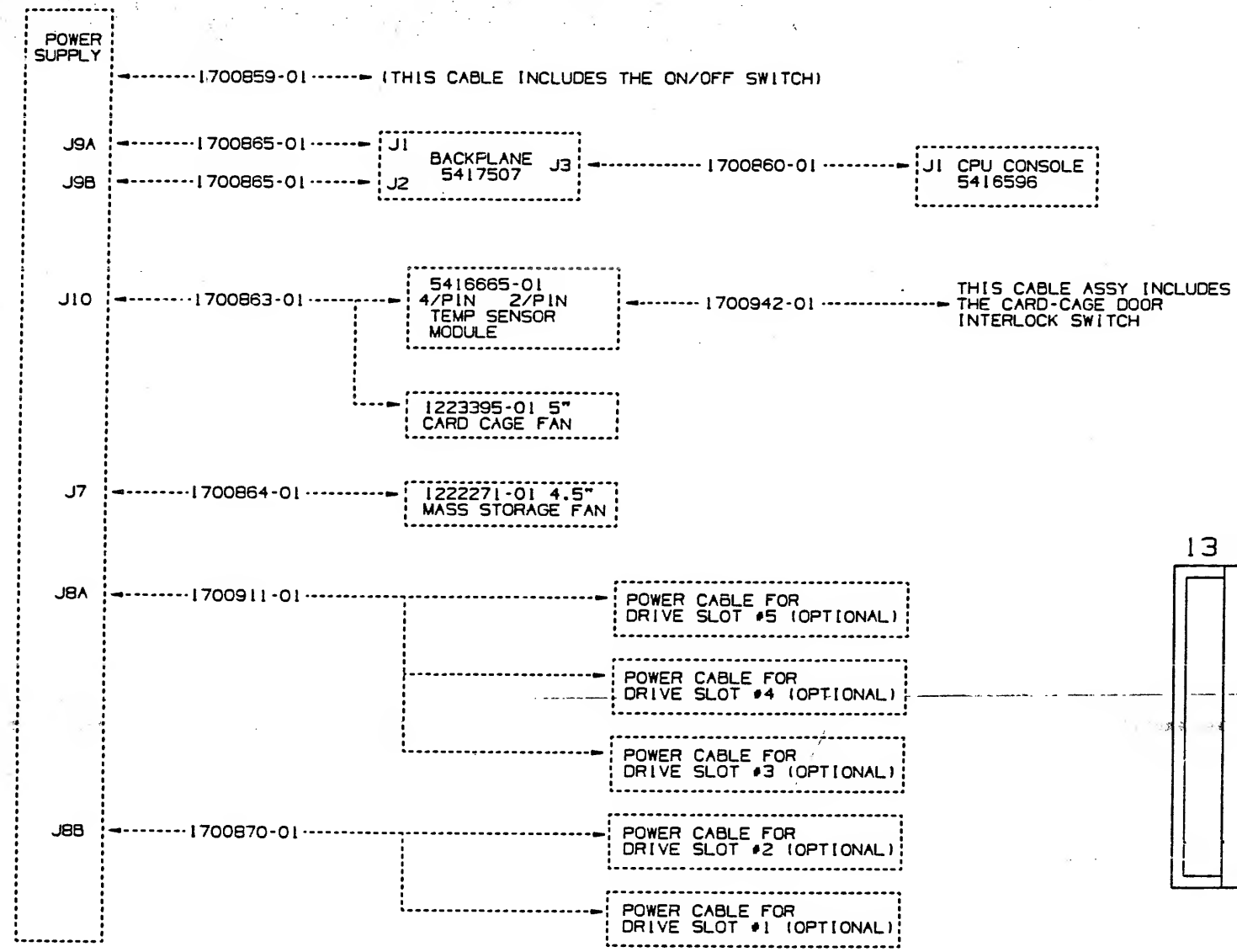
ML01

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NOTES: BACKPLANE CONFIGURATION RULES

WHEN CONFIGURING THE BACKPLANE, THE FOLLOWING RULES MUST BE REFERENCED:

1. ALL Q-BUS OPTIONS ARE INSTALLED BELOW THE CPU MODULE.
2. QUAD OPTIONS MAY BE INSTALLED ANYWHERE BELOW THE CPU MODULE.
3. DUAL OPTIONS CAN BE INSTALLED ANYWHERE BETWEEN SLOT 5-12 (i.e. AB OR CD ROWS) AND BETWEEN SLOT 1-4 ON THE AB ROWS BELOW THE CPU. NO DUAL OPTIONS MAY BE INSTALLED IN SLOTS 2 THROUGH 4 ON THE CD ROWS.
4. DUAL OPTIONS ALONE IN A SLOT REQUIRE A M9047 GRANT CARD ADJACENT TO THEM (A OR C ROWS).
5. SLOT 13 RESERVED FOR DIGITAL USE ONLY.



BA123-A BASIC ENCLOSURE POWER HARNESS WIRING DIAGRAM

BACKPLANE MODULE UTILIZATION- SEE RULES THIS SHEET

REVISIONS		
CHK	CHANGE NO	REV

TITLE BA123-A SYSTEM ARRANGEMENT		SIZE CODE D	NUMBER AR 7022380-0-DBU	REV A
SCALE 1/1	SHEET 6 OF 6	DIST		

PLOT AT 1.000

ML01

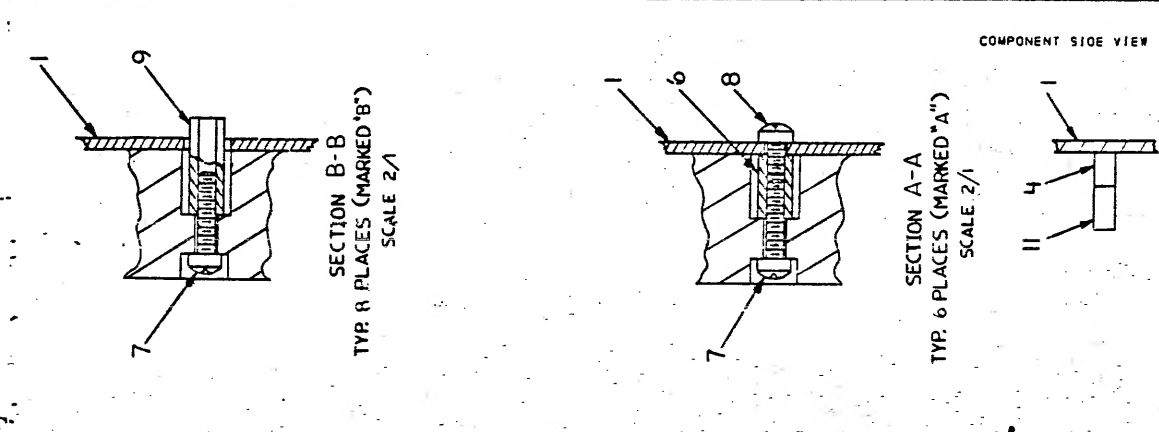
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LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY	PER VARIATION	REFERENCE DESIGNATOR
						01		
					VARIATION REVISION LEVEL:	A1		
1	1	D-MD-5017506-0-0	5017506-01		ETCHED BOARD	1		
2	2		1214886-05		PCB HEADER 10POS(2X 5).100CC	1		J2
3	3		1215699-07		PCB,HEADER 18POS(1X18).156CC STR	2		J1,J3
4	4		1217535-05		SKT,IC 13PIN SIP TIN SOLD	4		XZ1-XZ4
5	5		7417041-00		288 PIN CONNECTOR	6		J4-J9
6	6		9000033-12		SPACER,THREADED HEX ALUM 8-3	6		
7	7		9006120-06		SCREW, FILL POZI 8-	14		
8	8		9006035-01		SCREW,MACH PAN PHIL 8-	6		
9	9		9009246-00		SPACER,THREADED HEX ALUM 8-3	8		
10	10		7411881-01		DECAL	1		
11	11		1323505-01		R NETWORK 180/390 2.0 % 13PIN	4		Z1-Z4
12	12		7417042-00		72 PIN CONNECTOR	2		J10-J11
13	13		3623593-01		LABEL,BLANK,PAPER,PIN FEED	1		
14	14		9905016-03		CARTON,DIE CUT,SELF LOCK W/FOAM	1		

REVISION HISTORY			BASIC PART NO: 5417507		DRN: S.MANSOR		DATE: 07-JUN-84		D I G I T A L	
ENG	ECO NUMBER	REV	SECTION A OF A	CHK'D: F.GAROFALO	DATE: 1-MAR-85	TITLE PARTS LIST 13 SLOT BACKPLANE				
---	INITIAL	A	SECTION VARIATION INDEX	DES.ENG: T.ORR	DATE: 1-MAR-85	DOCUMENT NUMBER				
			[A] 01	RESP.ENG.: T.ORR	DATE: 1-MAR-85	SIZE	CODE	NUMBER	REV	
			[B]	MFG.ENG.: R.BELIVEAU	DATE: 1-MAR-85	K	PL	5417507-0-DBP	A	
			[C]	ASSEMBLY NUMBER:	TOP DOCUMENT NUMBER:	FILE NAME:				
			[D]	E-UA-5417507-0-0	B-DD-5417507-0-0	TW261A.PLS				
			[E]			RELEASE DATE: 04-MAR-85				
			[F]			EDIT #				
			[G]			4				
			[H]	"THIS DRAWING AND THE SPECIFICATIONS CONTAINED HEREIN ARE CONFIDENTIAL AND PROPRIETARY. THEY ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. THIS IS AN UNPUBLISHED WORK PROTECTED UNDER THE FEDERAL COPYRIGHT LAWS."						
			[I]							
			[J]							
			[K]							
			[L]							
			[M]							
			[N]							



CHIEF OF BUREAU
NO. 100



UK RATING IS MPWR.		STEP 1 1/4'S	
INSTALL J1, J2, J3 ON SIDE 2.		STEP 2 1/4'S	
REMOVE ITEM 8 (SOLDER LABELED X) AFTER		STEP 3 1/4'S	
WAVE SOLDER.		STEP 4 1/4'S	
STICK LABEL ON "J10"		STEP 5 1/4'S	
P E		STEP 6 1/4'S	
P E		STEP 7 1/4'S	
P E		STEP 8 1/4'S	
P E		STEP 9 1/4'S	
P E		STEP 10 1/4'S	
P E		STEP 11 1/4'S	
P E		STEP 12 1/4'S	
P E		STEP 13 1/4'S	
P E		STEP 14 1/4'S	
P E		STEP 15 1/4'S	
P E		STEP 16 1/4'S	
P E		STEP 17 1/4'S	
P E		STEP 18 1/4'S	
P E		STEP 19 1/4'S	
P E		STEP 20 1/4'S	
P E		STEP 21 1/4'S	
P E		STEP 22 1/4'S	
P E		STEP 23 1/4'S	
P E		STEP 24 1/4'S	
P E		STEP 25 1/4'S	
P E		STEP 26 1/4'S	
P E		STEP 27 1/4'S	
P E		STEP 28 1/4'S	
P E		STEP 29 1/4'S	
P E		STEP 30 1/4'S	
P E		STEP 31 1/4'S	
P E		STEP 32 1/4'S	
P E		STEP 33 1/4'S	
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P E		STEP 101 1/4'S	
P E		STEP 102 1/4'S	
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P E		STEP 104 1/4'S	
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P E		STEP 106 1/4'S	
P E		STEP 107 1/4'S	
P E		STEP 108 1/4'S	
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P E		STEP 111 1/4'S	
P E		STEP 112 1/4'S	
P E		STEP	

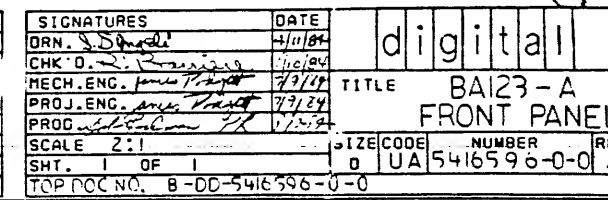
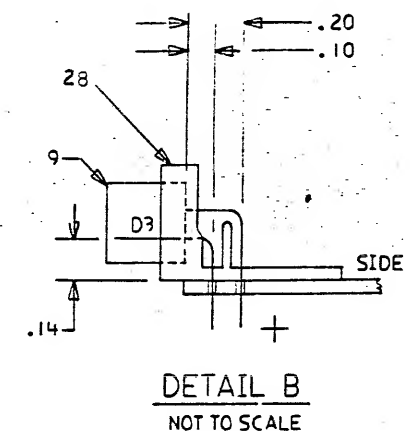
LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION		REFERENCE DESIGNATOR
						01	A2	
1	1	D-MD-5016595-0-0	5016595-01		CIRCUIT DRILL AND ETCH	1		
2	2		1000021-00		220.0 MMF 100V 5%200PPM MICA	1		C1
3	3		1005636-00		22 MFD 6V 10% S.TANT	1		C2
4	4		1012784-00		.047 MFD 50V +80-20% CER	2		C3,C4
5	5		1012312-01		.47 MFD 50V +90-20% CER	1		C5
6	6		1017472-00		10 MFD 35V +75-10% AL EL	1		C6
7	7		1100114-00		PIV= 25 IO=135 MA	1		D1
8	8		1119827-01		LED,SUPERBRIGHT,RED T1 PKG	1		D2
9	9		1116622-02		LED 2.0MCD@25M	1		D3
10	10		1121248-01		GREEN LED T1 4MCD 1"LEADS	1		D4
11	11		1110864-00		LED 2MCD@10MA	2		D5,D6
12	12		1218945-03		SW,PB,LT 1PST NO-MOMENTARY .25A	1		S1
13	13		1218945-01		SW,PB,LT 1PST NO-MAINTAIN .25A	1		S2
14	14		1217310-07		SW,DIP 2POS/1PST 5VDC100MA S	1		S3
15	15		1216832-07		*** THIS ITEM IS NOT USED ***	-		
16	16		1219918-01		SKT,SWITCH 4PIN RT ANGLE	2		XS1,XS2
17	17		1300250-00		150.0 .25 W 5.0 % CF	1		R1
18	18		1311523-00		110.0 .25 W 5.0 % CF	1		R2
19	19		1300271-00		220.0 .25 W 5.0 % CF	1		R3
20	20		1302388-00		2.0 K .25 W 5.0 % CF	4		R4,R5,R6,R7
21	21		1300479-00		10.0 K .25 W 5.0 % CF	4		R10-R13
22	22		1302514-00		39.0 K .25 W 5.0 % CF	2		R14,R15
23	23		1302466-00		100.0 K .25 W 5.0 % CF	1		R16
24	24		1300391-00		1.50 K .25 W 5.0 % CF	2		R8,R9
25	25		1914987-00		8641-2 TRANSCEIVER,UNIBUS,QU	1		E1
26	26		1912858-00		LS221 ONE SHOT-DUAL,SCHMIT	1		E2
27	27		1914156-01		LM 393AN VOLT COMPARATOR,DUA	1		E3
28	28	D-MD-7430089-0-DBU	7430089-01		HOLDER,L.E.D.,SINGLE	1		
29	29		1209941-05		PCB,HEADER 10PIN(2X10).100CC 90D	1		J1
30	30		1209941-04		PCB,HEADER LATCH	1		

REVISION HISTORY			BASIC PART NO: 5416596			D I G I T A L		
ENG	ECO NUMBER	REV	SECTION A - OF A	DRN:	M. FUNARO	DATE: 16-MAR-84		
JP	INITIAL	A	SECTION VARIATION INDEX	CHK'D:	D. BARRIERE	DATE: 16-MAR-84	TITLE PARTS LIST	
JP	5416596-ML001	B	(A) 01				BA123-A FRONT PANEL	
			(B)	DES.ENG:	J. PADGETT	DATE: 16-MAR-84	DOCUMENT NUMBER	
			(C)				SIZE	CODE
			(D)	RESP.ENG.:	J. PADGETT	DATE: 16-MAR-84	NUMBER	
			(E)				K	PL
			(F)	MFG.ENG.:	R. BELIVEAU	DATE: 18-MAY-84	RELEASE DATE: 01-MAY-85	
			(H)					
			(J)	ASSEMBLY NUMBER:	D-UA-5416596-0-0	TOP DOCUMENT NUMBER:	FILE NAME:	EDIT #
			(K)				B-DD-5416596-0-0	29241B.PLS
			(L)					
			(M)					
			(N)					

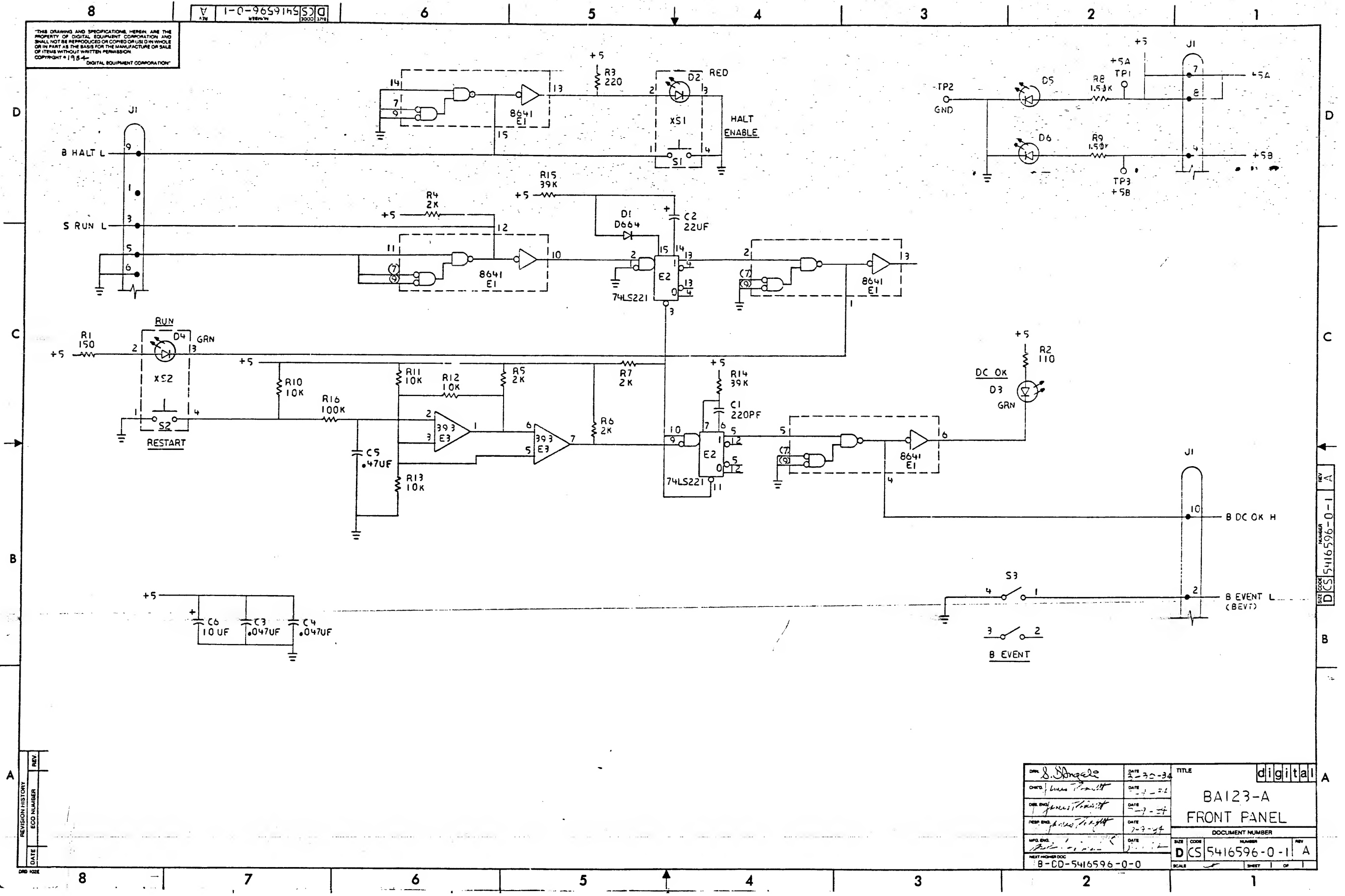
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LINE ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION 01 A2	REFERENCE DESIGNATOR
31	31	1209941-03		PCB,HEADER LATCH	1	

DIGITAL	TITLE	BA123-A FRONT PANEL	SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
				K	PL	5416596-0-DBP	B



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REV	ECO NUMBER	DATE
1		

DATE	2-20-84	TITLE	digital
CHG'D	Wm. T. Smith	DATE	2-20-84
CHK'D	James T. Smith	DATE	2-20-84
TRSP. ENG.	James T. Smith	DATE	2-20-84
WFO. ENG.	James T. Smith	DATE	2-20-84
NEXT HIGHER DOC	B-CD-5416596-0-0	DOCUMENT NUMBER	BA123-A FRONT PANEL
SIZE	CODE	NUMBER	REV
D	CS	5416596-0-1	A
SCALE	SHEET	OF	

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DRAWING DIRECTORY

ITEM	DRAWING NO.	NO. OF SHTS	PART NO.	DESCRIPTION	TYPE	REVISIONS											
						A1	A1	A2									
1			5416665-01	TEMP SENSOR BD.		A1	A1	A2									
2	D-UA-5416665-0-0	1		TEMP SENSOR BD.		A	B	C									
3	D-CS-5416665-0-1	1		TEMP SENSOR BD.		A	A	A									
4	K-PL-5416665-0-DBP	1		TEMP SENSOR BD.		A	A	B									
5	K-PC-5416665-0-DBC			P.C. DESIGN DATA BASE		A	A	A									
6			5016664-01	ETCHED CIRCUIT BOARD		B1	B1	B1									
7	B-DD-5016664-0-0	1		DRAWING DIRECTORY		A	A	A									
NOTES:					DD REV	A	B	C									
REVISION HISTORY			CONT. REVISION HISTORY			MADE BY: P.LENNON DATE: 23-OCT-84			d i g i t a l								
ENG	ECO NUMBER	REV	ENG	ECO NUMBER	REV	CHECKED BY: D. BARRIERE DATE: 23-OCT-84			TITLE DRAWING DIRECTORY								
TO	INITIAL	A				DESIGN ENGINEER: T. ORR DATE: 23-OCT-84			TEMP SENSOR BD.								
RL	5416665-ML001	B				RESPONSIBLE ENG: R. LIGENZA DATE: 04-FEB-86											
	5416665-MK002	C				PRODUCTION ENG: NEMI HARRIS DATE: 04-FEB-86			SIZE K CODE DD DOCUMENT NUMBER K-DD-5416665-0 REV. C								
									SHEET 1 OF 1 MKO								

AUTOMATED BY VAXKPL (V1.0)

PARTS LIST

SHEET A1 OF A1

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VAR/REV	REFERENCE DESIGNATORS
						01	
						A2	
1	1	D-MD-5016664-0-0	50-16664-01		CIRCUIT DRILL & ETCH	1	
2	2		13-24146-01		*** THIS ITEM IS NOT USED ***	-	
3	3		12-23681-03		THERMOSTAT, NO C3 50C	1	
4	4		12-11342-04		MATE-N-LOK 04PIN(1X04).200CC HDR	1	TS1
5	5		12-11342-02		MATE-N-LOK 02PIN(1X02).200CC HDR	1	J1
6	6		90-07254-00		TRANSIPADS #10146	2	J2
7	7		13-25634-01 A		THERMISTOR, EPOXY COATED, 50J0HM 5	1	R1

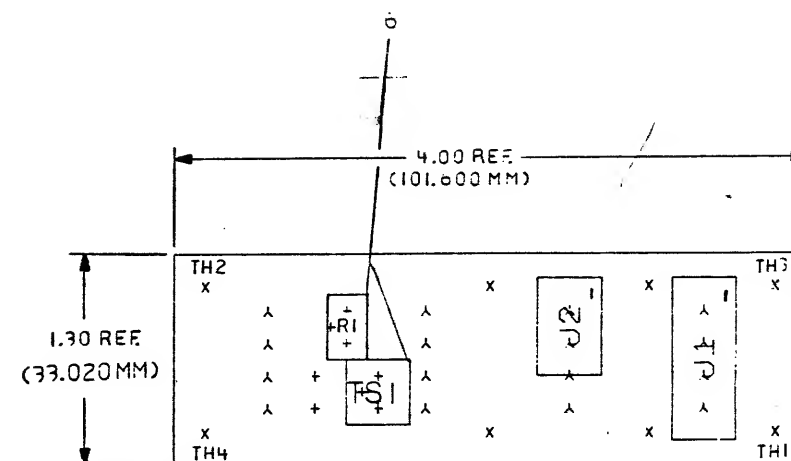
REVISION HISTORY			KPL MODULE FORMAT		SECTION A OF A		DRN: T. ORR	
ENG	ECO NUMBER	REV	SECTION/VARIATION INDEX		DATE: 25-OCT-84		D I G I T A L	
TO	INITIAL	A	[A]	01	[M]	CHK'D: D. BARRIERE	TITLE PARTS LIST	
RL	5416665-MK002	B	[B]		[N]	DATE: 25-OCT-84	TEMP SENSOR BD	
			[C]		[P]	DES.ENG: T. ORR		
			[D]		[Q]	DATE: 25-OCT-84		
			[E]		[R]	RESP.ENG: T. ORR	DOCUMENT NUMBER	
			[F]		[S]	DATE: 25-OCT-84	SIZE	CODE
			[G]		[T]		NUMBER	REV
			[H]		[U]		K	PL
			[I]		[V]		5416665-0-D3P	B
			[J]		[W]			
			[K]		[X]			
			[L]		[Y]			
			BASIC PART NUMBER: 5416665		ASSEMBLY NUMBER: D-UA-5416665-0-0		TOP DOCUMENT NUMBER: B-DD-5416665-0-0	
							FILE NAME: MK1283.PLS	
							EDIT # 2	
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NOTES:
1: ON SIDE ONE, IDENTIFY POINT OF MANUFACTURE, DATE CODE AND REVISION

STEP	E	Y AXIS	STEP	TIMES
REPEAT		X AXIS	STEP	TIMES

CHG	NO	REV	INIT	DATE
1084		A		
54665		B		
ML001				
6/85		WEINBERG		
J		PADGETT		
6/88		F214		
PHASE 3 MODE C				
A. KRAVETSKY				
R. L. GENZA				
J. W. J. (2)				

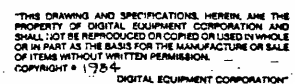


ETCH REV. B1

SIGNATURES	DATE
DRN. J. W. J.	12/24
CHK'D. J. W. J.	12/24
MECH. ENG. J. W. J.	12/24
PROJ. ENG. J. W. J.	12/24
PROD. J. W. J.	12/24
SCALE 2:1	
SHT. 1 OF 1	
TOP D.C. NO. 8-00-541665-0-0	

TITLE	TEMP
SENSOR BD.	
SIZE CODE	NUMBER
0 1A	541665-0-0 C

1 MS# 18-6928



DATE	2.8.89	DATE	24 OCT 84	TITLE	digital			
CHRG	D. Brune	DATE	24 OCT 84	TEMP				
DEL ENCL	J. Prigent	DATE	13 OCT 84	SENSOR BD				
REP ENCL	J. Prigent	DATE	13 OCT 84	DOCUMENT NUMBER				
WFO ENCL	A. L. Lemaire	DATE	2.11.84	SIZE	CODE	MESSAGE	REF.	
HEAVY DUTY TOP DOC NO.			D		C	S	A	
B-DD-5416665-0			SCALE	1/1	SHEET	OF		